88F5281

Feroceon® SoC

Datasheet

Doc. No. MV-S103889-00, Rev. E
April 29, 2008, Preliminary

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

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PRODUCT OVERVIEW

The Marvell® 88F5281 device is a high-performance integrated controller. It is based on the Marvell Feroceon® CPU core, which is compliant with the ARMv5TE. The device is intended for use in a wide range of systems with extensive communication and connectivity requirements.

FEATURES

- **High performance integrated controller**
  - High performance Feroceon 88FR531-vd dual issue CPU with Vector Floating Point (VFP) support
  - High bandwidth dual-port memory controller (16-/32-bit DDR1/DDR2 SDRAM)
  - Single PCI Express (x1) port with integrated PHY
  - Single 64-bit PCI2.2/PCI-X 133 MHz port
  - Single Gigabit Ethernet MAC (10/100/1000 Mbps)
  - Single USB2.0 peripheral or host port with integrated PHY
  - Two-Wire Serial Interface (TWSI)
  - 2 UART ports
  - 32-bit device bus with up to 4 chip selects
  - NAND Flash support
  - Integrated DMA engine (4 channels)
  - 20 multi-purpose pins
  - Interrupt controller
  - Timers
- **Feroceon 88FR531-vd dual issue CPU with VFP support**
  - Up to 500 MHz
  - Super scalar, dual issue CPU
  - Single precision and double precision VFP support
  - 32-bit and 16-bit RISC architecture
  - Compliant with v5TE architecture, published in the *ARM Architecture Reference Manual*, Second Edition
  - Supports 32-bit instruction set for performance and flexibility
  - Supports 16-bit Thumb instruction set for code density
  - Supports DSP instructions to boost performance for signal processing applications
  - Includes MMU to support virtual memory features
  - MPU can be used instead when not using MMU
  - 32-KByte I-Cache and 32-KByte D-Cache
  - 64-bit internal data bus
  - Variable pipeline stages—six to nine stages
  - Out-of-order execution for increased performance
  - In-order retire via a Reordering Buffer (ROB)
  - Branch Prediction Unit
  - Supports JTAG/ARM-compatible ICE
  - Supports both Big and Little Endian modes
- **DDR1/DDR2 SDRAM controller**
  - DDR SDRAM with a clock ratio of 1:2 or 1:3 between the DDR SDRAM and the Feroceon core, respectively
  - 16-bit/32-bit interface
  - DDR1 at up to 166 MHz
  - DDR2 at up to 200 MHz
  - Supports up to two dual sided DIMMs
  - Supports DDR components of x8 and x16
  - Dual channel memory controller
    Reduced CPU to DDR SDRAM latency
  - SSTL 2.5V I/Os in DDR1, 1.8V I/Os in DDR2
  - Supports four DDR SDRAM banks (CSs)
  - DDR1 supports device densities of 128, 256, and 512 Mb
  - DDR2 supports device densities of 256 and 512 Mb
  - Up to 1 GB (32-bit interface) and 0.5 GB (16-bit interface) total memory space
  - Supports DDR SDRAM bank interleaving between all DDR SDRAM banks (both the physical banks and the four internal banks of the DDR SDRAM devices)
  - Supports up to 16 open pages (page per bank)
  - Supports configurable DDR SDRAM timing parameters
  - Supports up to 32-byte burst per single DDR SDRAM access
  - Single ended DQS in DDR2
  - DDR1/DDR2 pad auto calibration
  - Supports DDR2 On Die Termination (ODT)

- **PCI Express interface (x1)**
  - PCI Express Base 1.0a compatible
  - Integrated low power SERDES PHY, based on Marvell SERDES technology
  - Root Complex Port
  - Can also be configured as an Endpoint port
  - x1 link width
  - 2.5 GHz signalling
  - Lane polarity reversal support
  - Maximum payload size of 128 bytes
  - Single Virtual Channel (VC-0)
  - Replay buffer support
  - Extended PCI Express configuration space
  - Advanced Error Reporting (AER) support
  - Power management: L0s and SW L1 support
  - Interrupt emulation message support
  - Error message support
- **PCI Express master specific features**
  - Single outstanding read transaction
  - Maximum read request of up to 128 bytes
  - Maximum write request of up to 128 bytes
  - Up to four outstanding read transactions in Endpoint mode
- **PCI Express target specific features**
  - Supports up to eight read request transactions
  - Maximum read request size of 4 KB
  - Maximum write request of 128 bytes
  - Supports PCI Express access to all of the device's internal registers
- **64-bit PCI/PCI-X Interface**
  - 66 MHz PCI 2.2 compliant interface
  - 133 MHz PCI-X compliant interface
  - 3.3V I/Os, 5V tolerant
  - Supports 64-bit addressing via DAC transactions
  - Configurable PCI arbiter for up to six masters
- **PCI/PCI-X master specific features**
  - Supports all PCI and PCI-X cycles
  - Host to PCI bridge—translates CPU cycles to PCI Memory, I/O, or configuration cycles
  - Supports DMA bursts between PCI and memory
  - Supports transaction combining to unlimited PCI burst (conventional PCI)
  - Supports up to four outstanding split transactions (PCI-X)
- **PCI/PCI-X target specific features**
  - Supports all PCI and PCI-X cycles
  - Supports programmable aggressive read prefetch (conventional PCI)
  - Supports up to 4 KB read per single transaction (PCI-X)
  - Supports unlimited burst write with zero wait states
  - Supports up to four delayed reads (conventional PCI)
  - Supports up to four split reads (PCI-X)
  - Supports PCI access to all of the device's internal registers
  - PCI address remapping to local memory
- **PICMG Compact PCI Hot-Swap ready**
- **PCI/PCI-X "Plug and Play" support**
  - Plug and Play compatible configuration registers
  - PCI configuration registers that are accessible from both the Feroceon CPU core and PCI
  - Vital Product Data (VPD) support
  - PCI Power Management (PMG) support
  - Message Signal Interrupts (MSI) support
- **Integrated Single GbE (10/100/1000) MAC**
  - Supports 10/100/1000 Mbps
  - MII, GMII or RGMII Interface
  - Proprietary 200 Mbps Marvell MII (MMII) interface
  - Dedicated DMA for data movement between memory and port
  - Priority Queuing on receive based on DA, VLAN Tag, and IP TOS
  - Layer 2/3/4 frame encapsulation detection
  - TCP/IP checksum on receive and transmit
  - DA address filtering
- **USB2.0 Peripheral or Host port**
  - USB 2.0 compliant
  - Integrated USB 2.0 PHY
  - EHCI compatible as a host
  - As a host, supports direct connection to all peripheral types (LS, FS, HS)
  - As a peripheral, connects to all host types (HS, FS) and hubs
  - Up to 4 independent endpoints supporting control, interrupt, bulk, and isochronous data transfers
  - Dedicated DMA for data movement between memory and port
- **Two-Wire Serial Interface (TWSI)**
  - Master/slave operation
  - Serial ROM initialization
- **Two UART interfaces**
  - 16550 UART compatible
  - Two pins for transmit and receive operations
  - Two pins for modem control functions

- **Device Bus Controller**
  - 8-/16-/32-bit width
  - 166 MHz clock frequency
  - 3.3V I/Os
  - Supports many types of standard memory devices such as FLASH, ROM, and SyncBurst SRAM
  - Four chip selects with programmable timing
  - Optional external wait-state support
  - Boot ROM support
- **NAND Flash support**
  - Glueless interface to CE don't care NAND Flash through the device bus interface
  - Glueless interface to CE care NAND Flash through the device bus and MPP interfaces
  - Boot from NAND Flash when the 1st block, placed on 00h block address, is guaranteed to be a valid block with no errors
  - Supports read bursts of up to 128 bytes
- **Four channel Independent DMA controller**
  - Chaining via linked-lists of descriptors
  - Moves data from any to any interface
  - Supports increment or hold on both source and destination address
- **20 multi-purpose pins dedicated for peripheral functions and general purpose I/O**
  - Each pin can be configured independently
  - GPIO inputs can be used to register interrupts from external devices and to generate maskable interrupts
- **Interrupt controller**
  - Maskable interrupts to Feroceon core
  - In endpoint mode, maskable interrupts to PCI/PCI Express interfaces
- **Timers**
  - Two general purpose 32-bit timer/counters
  - One 32-bit Watchdog timer
- **Internal Architecture**
  - Mbus-L bus for high-performance, low latency Feroceon CPU core to DDR SDRAM connectivity
  - Advanced Mbus (crossbar extension) architecture with any to any concurrent IO connectivity
  - Dual port DDR SDRAM controller connectivity to both CPU and Mbus
- **Bootable from:**
  - Device interface, including glueless boot from NAND flash
  - PCI Express interface
  - PCI interface
- **HSBGA, 23x23 mm, 426-pin package, 1 mm ball pitch**

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Preface

About This Document

This datasheet provides the hardware specifications for the Marvell® 88F5281 Feroceon® SoC. The hardware specifications include detailed pin information, configuration settings, electrical characteristics, and physical specifications.

This document is intended to be the basic source of information for designers of new systems.

Related Documentation

The following documents contain additional information related to the 88F5281:

- *88F5281 Feroceon® SoC User Manual*, Doc. No. MV-S103890-00
- *88F5281 Feroceon® SoC Functional Errata, Guidelines, and Restrictions*, Doc. No. MV-S500832-00
- *Orion SoC Hardware Design Guide,* Doc. No. MV-S103315-00[1]
- *ARM Architect Reference Manual*, Second Edition
- *PCI Local Bus Specification*, Revision 2.2
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b
- *PCI Express Base Specification*, Revision 1.1
- *Universal Serial Bus Specification, Revision 2.0*, April 2000, Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips http://www.usb.org
- *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 0.95, November 2000, Intel Corporation http://www.intel.com
- *USB-HS High-Speed Controller Core* reference[1]
- *AN-123 Power Sequencing for Marvell Devices,* Doc. No. MV-S300427-00[1]

See the Marvell Extranet website for the latest product documentation.

1. This document is a Marvell proprietary confidential document requiring an NDA and can be downloaded from the Marvell Extranet.

Document Conventions

The following conventions are used in this document.

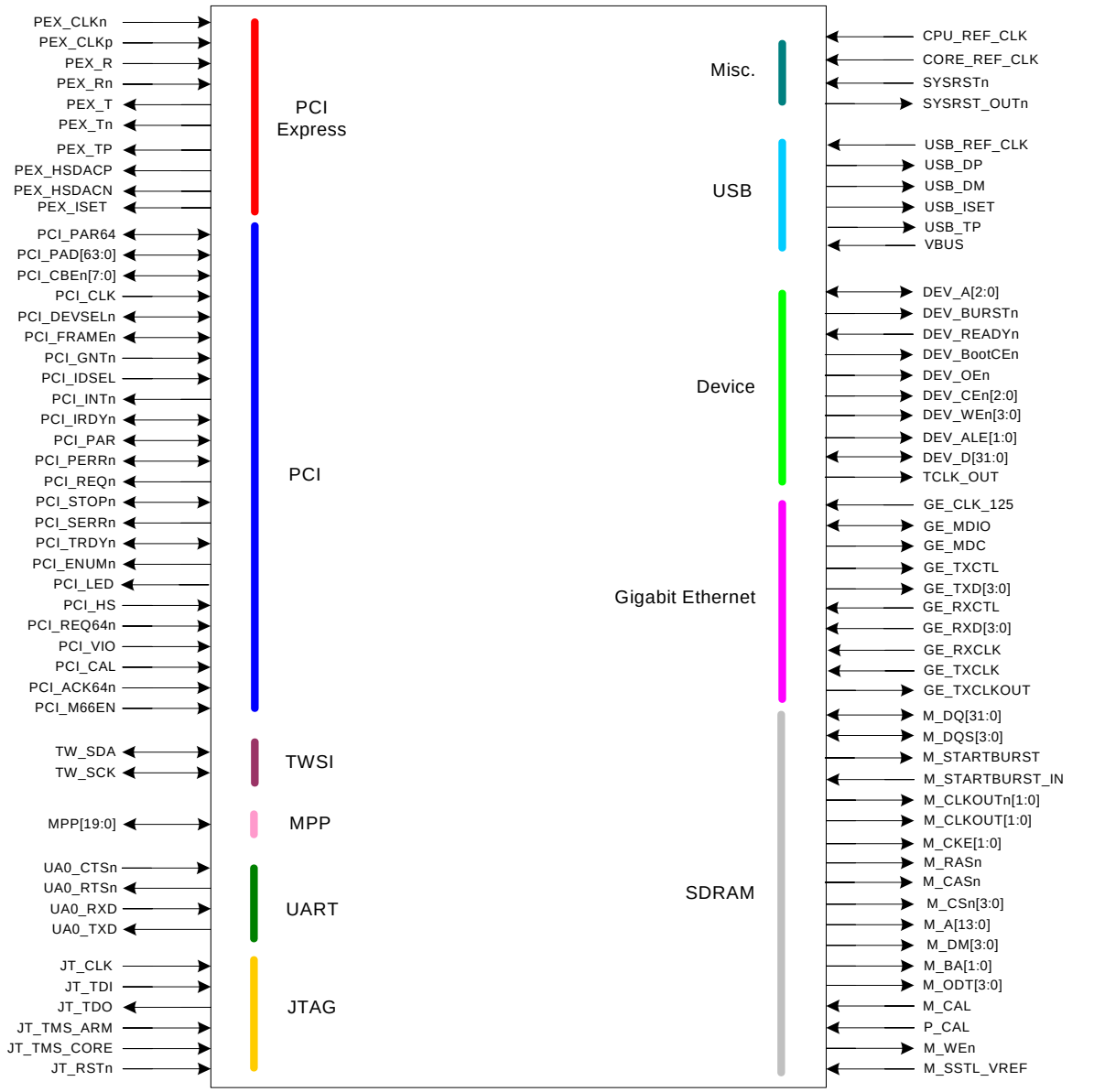
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_AD[31:0]
Active Low Signals n	A "n" symbol at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated in courier font. Example: <Dwidth> OR Example: SDRAM_Configuration<Dwidth>, Where **SDRAM Configuration** represents the register name, and <Dwidth> represents the register field name. Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use.

1 Pin Descriptions

This section provides the pin logic diagram for each packet processor and a detailed description of the pin assignments and their functionality.

1.1 Pin Logic

Figure 1: 88F5281 Pin Logic Diagram



1.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 1 defines the abbreviations and acronyms used in the pin description tables.

Table 1: Pin Assignment Table Conventions

Abbreviation	Description
I	Input
O	Output
I/O	Input/Output
t/s	Tri-State pin.
s/t/s	Sustained Tri-State pin. The pin is driven to its inactive value for one cycle before float. A pull-up is required to sustain the inactive value.
o/d	Open Drain pin. The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
SDR	Single Data Rate
DDR	Double Data Rate
CML	Current Mode Logic
LVTTL	Low-voltage TTL 3.3V Driver/Receiver
LVCMOS	Low-voltage CMOS 2.5V Driver/Receiver
HCSL	High-speed Current Steering Logic
HSTL	High Speed Transceiver Logic 1.5V Pad
SSTL_2	Stub Series Terminated Logic for 2.5V Pad
PCI	PCI pad 3.3V according to the PCI standard
n	Represents the port number
Calib	Calibration pad type
Power	VDD Power Supply
GND	Ground Supply
Analog	Analog Supply
VREF	Reference Voltage

Table 2: Interface Pin Prefixes

Interface	Prefix
DDR SDRAM	M_
PCI Express	PEX_
PCI/PICE-X	PCI_
Gigabit Ethernet	GE_
USB 2.0	USB_
TWSI	TW_
UART 0	UA0_
Device Bus	DEV_
MPP	N/A
JTAG	JT_
Misc	N/A

1.2.1 DDR SDRAM Interface Pin Assignments

Table 3: DDR SDRAM Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
M_SSTL_VREF	I	VREF	VDD_M	SSTL Reference Voltage 0 Reference voltage for SSTL interface (1.25V for DDR1, 0.9V for DDR2)
M_CLKOUT[1:0] M_CLKOUTn[1:0]	O	SSTL	VDD_M	SDRAM Clock Differential SDRAM clock pairs
M_CKE[1:0]	O	SSTL	VDD_M	SDRAM Clock Enable Driven high to enable SDRAM clock. Driven low when putting the SDRAM in self refresh mode.
M_RASn	O	SSTL	VDD_M	SDRAM Row Address Select Asserted to indicate an active ROW address driven on the SDRAM address lines.
M_CASn	O	SSTL	VDD_M	SDRAM Column Address Select Asserted to indicate an active column address driven on the SDRAM address lines.
M_WEn	O	SSTL	VDD_M	SDRAM Write Enable Asserted to indicate a write command to the SDRAM.
M_A[13:0]	O	SSTL	VDD_M	SDRAM Address Driven during RASn and CASn cycles to generate, together with the bank address bits, the SDRAM address.
M_BA[1:0]	O	SSTL	VDD_M	SDRAM Bank Address Driven during RASn and CASn cycles to select one of the four SDRAM virtual banks.
M_CSn[3:0]	O	SSTL	VDD_M	SDRAM Chip Selects Asserted to select a specific SDRAM bank.
M_DQ[31:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Bus Driven during write to SDRAM. Driven by SDRAM during reads.
M_DQS[3:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Strobe • DQS[0] is the strobe for DQ[7:0]. • DQS[1] is the strobe for DQ[15:8]. • DQS[2] is the strobe for DQ[23:16]. • DQS[3] is the strobe for DQ[31:24]. Driven during write to SDRAM. Driven by SDRAM during reads.
M_DM[3:0]	O	SSTL	VDD_M	SDRAM Data Mask • DM[0] is the mask for DQ[7:0]. • DM[1] is the mask for DQ[15:8]. • DM[2] is the mask for DQ[23:16]. • DM[3] is the mask for DQ[31:24].

Table 3: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
M_STARTBURST	O	SSTL	VDD_M	Start Burst Indication of burst start Indicates the entire window of the read transaction. It is a Marvell® proprietary signal. Routes M_STARTBURST signal to the 88F5281 as M_STARTBURST_IN. Refer to the *Orion SoC Hardware Design Guide* for layout considerations.
M_STARTBURST_IN	I	SSTL	VDD_M	Start Burst Input
M_ODT[3:0]	O	SSTL	VDD_M	SDRAM On Die Termination control Turns on/off SDRAM on die termination resistor. Pin per each SDRAM chip select
M_CAL	I	Calib		SDRAM Auto Calibration input Allows control of the DDR SDRAM interface output buffers' strength. Connect this pin to VDD_M through a resistor. The resistor value determines the drive strength of the output buffer. Refer to the *Hardware Design Guidelines* for this product and also refer to the product's development board schematics.
P_CAL	I	Calib		SDRAM Auto Calibration input for the P-channel transistor only Allows control of the DDR SDRAM interface output buffers' strength. Connect this pin to VSS through a resistor. The resistor value determines the drive strength of the output buffer. Refer to the *Hardware Design Guidelines* for this product and also refer to the product's development board schematics.
VDD_M	I	Power		DDR1/DDR2 SDRAM Interface I/O Supply Voltage

1.2.2 PCI Express Interface Pin Assignments

Table 4: PCI Express Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
PEX_CLKp, PEX_CLKn	I	HCSL	PEX_AVDD	PCI Express Reference Clock Input 100 MHz, differential
PEX_T, PEX_Tn	O	CML	PEX_AVDD	Transmit Lane Differential pair of PCI Express transmit data
PEX_R, PEX_Rn	I	CML	PEX_AVDD	Receive Lane Differential pair of PCI Express receive data
PEX_HSDACP PEX_HSDACN	O	CML	PEX_AVDD	High Speed DAC
PEX_ISET	O	Analog	PEX_AVDD	Current Reference Tie to VSS through a 6.04 kilohm (1%) resistor.
PEX_TP	O	Analog	PEX_AVDD	Analog Test Point
PEX_AVDD	I	Power		PCI Express PHY quiet power supply
PEX_AVDDL	I	Power		PCI Express PHY quiet power supply
PEX_AVDDT	I	Power		PCI Express PHY quiet power supply

1.2.3 PCI Bus Interface Pin Assignments

Table 5: PCI Bus Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
PCI_CLK	I	PCI	VDDO	PCI Clock PCI interface clock (up to 133 MHz in PCI-X mode and up to 66 MHz in conventional PCI mode)
PCI_VIO	I	PCI	VDDO	PCI VIO Clamping reference voltage for PCI (3.3V or 5V
PCI_M66EN	I	PCI	VDDO	PCI 66 MHz Enable **NOTE:** Only relevant for conventional PCI mode. If configured to PCI-X, the PCI interface internal DLL is enabled regardless of PCI_M66EN). PCI_M66EN is sampled on reset de-assertion, to determine if it is connected to a 66 MHz bus. If PCI_M66EN is sampled HIGH, the internal PCI interface DLL is enabled.
PCI_PAD[63:0]	t/s I/O	PCI	VDDO	PCI Address/Data 64-bit PCI multiplexed address/data bus. Driven by the transaction master during address phase and write data phase. Driven by the target device during read data phase.
PCI_CBEn[7:0]	t/s I/O	PCI	VDDO	PCI Command/Byte Enable 8-bit multiplexed command/byte-enable bus, driven by transaction master. Contains the command during the address phase and byte-enable during data phase.
PCI_PAR	t/s I/O	PCI	VDDO	PCI Parity (low) Even parity is calculated for PCI_PAD[31:0] and PCI_CBEn[3:0]. Driven by the transaction master for the address phase and the write data phase. This pin is driven by the target for the read data phase.
PCI_FRAMEn	s/t/s I/O	PCI	VDDO	PCI Frame Asserted by the transaction master to indicate the beginning of a transaction. The master de-asserts PCI_FRAMEn to indicate that the next data phase is the final data phase transaction.
PCI_IRDYn	s/t/s I/O	PCI	VDDO	PCI Initiator Ready Asserted by the transaction master to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_DEVSELn	s/t/s I/O	PCI	VDDO	PCI Device Select Asserted by the target of the current access. As a master, the target device is expected to assert PCI_DEVSELn within five bus cycles. Otherwise, it aborts the cycle. As a target, PCI_DEVSELn is asserted at a medium speed; two cycles after the assertion of PCI_FRAMEn.

Table 5: PCI Bus Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
PCI_STOPn	s/t/s I/O	PCI	VDDO	PCI Stop Asserted by target to indicate transaction termination. Used by a target device to generate a Retry, Disconnect, or Target Abort termination signal.
PCI_TRDYn	s/t/s I/O	PCI	VDDO	PCI Target Ready Asserted by the target to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_REQ64n	t/s I/O	PCI	VDDO	PCI Request 64-bit Transfer When configured to a 64-bit PCI bus, asserted by the transaction master to indicate a request of a 64-bit bus width transaction. PCI_REQ64n timing is the same as PCI_FRAMEn timing. A 64-bit transaction occurs when PCI_REQ64n and PCI_ACK64n are asserted.
PCI_ACK64n	t/s I/O	PCI	VDDO	PCI Acknowledge 64-bit Transfer When configured to a 64-bit bus, asserted by the target in response to PCI_REQ64n to indicate it accepts a 64-bit bus width transaction. PCI_ACK64n timing is the same as PCI_DEVSELn timing. A 64-bit transaction occurs when PCI_REQ64n and PCI_ACK64n are asserted.
PCI_PAR64	t/s I/O	PCI	VDDO	PCI Parity (high) In cases of a 64-bit PCI transaction, even parity is calculated for PCI_AD[63:32] and PCI_CBE[7:4]. Driven by the transaction master for address phase and write data phase. Driven by the target for read data phase.
PCI_IDSEL	I	PCI	VDDO	PCI Initialization Device Select Asserted to act as a target device chip select during PCI configuration transactions.
PCI_REQn/PCI_GNTn[1]	t/s O	PCI	VDDO	PCI Bus Request When using an external PCI arbiter, this pin is asserted to request PCI bus mastership to initiate a new transaction.
				PCI Device1 Grant When using the internal PCI Arbiter, the internal PCI controller is connected as agent0, and this pin functions as PCI Arbiter Grant for Agent1.
PCI_GNTn/PCI_REQn[1]	I	PCI	VDDO	PCI Bus Grant When using an external PCI arbiter, this pin is asserted to indicate that bus mastership is granted.
				When using the internal PCI Arbiter, the internal PCI port is connected as agent0, and this pin functions as PCI Arbiter Request of Agent1.
PCI_PERRn	s/t/s I/O	PCI	VDDO	PCI Parity Error Asserted when a data parity error is detected. Asserted by a target device in response to bad address or write data parity, or by master device in response to bad read data parity.

Table 5: PCI Bus Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
PCI_SERRn	o/d O	PCI	VDDO	PCI System Error Asserted when a serious system error (not necessarily a PCI error) is detected.
PCI_INTn	o/d O	PCI	VDDO	PCI Interrupt Request Asserted when one of the unmasked internal interrupt sources is asserted. If MSI is enabled, PCI_INTn is not asserted.
PCI_CAL	I	PCI	VDDO	PCI Auto Calibration input. Tie to VDDO through a reference resistor externally).
PCI_HS	I	PCI	VDDO	CompactPCI Handle Switch Compact PCI Hot Swap Handle Switch Sampled handle switch status to identify board insertion or removal.
PCI_ENUMn	o/d O	PCI	VDDO	CompactPCI ENUM interrupt Compact PCI Hot Swap ENUMn interrupt. If ENUM is enabled, this pin is asserted during Hot Swap insertion or removal.
PCI_LED	t/s O	PCI	VDDO	CompactPCI LED On/Off Compact PCI Hot Swap LED turn on/off.
PCI_AVDD	I	Power		PCI DLL quiet power supply 1.2V
PCI_AVSS	I	GND		PCI DLL quiet VSS

Note All PCI pads are 5V tolerant when PCI_VIO is conncted to 5V.

1.2.4 Gigabit Ethernet Port Interface Pin Assignments

Table 6: Gigabit Ethernet Port Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE_TXCLKOUT	t/s O	LVCMOS/ LVTTL	VDD_GE	RGMII Transmit Clock RGMII transmit reference output clock for GE_TXD[3:0] and GE_TXCTL Provides 125 MHz, 25 MHz or 2.5 MHz clock. Not used in MII mode
				GMII Transmit Clock Provides the timing reference for the transfer of the GE_TXEN, GE_TXERR, and GE_TXD[7:0] signals. This clock operates at 125 MHz.
GE_TXCLK	I	LVCMOS/ LVTTL	VDD_GE	MII Transmit Clock MII transmit reference clock from PHY. Provides the timing reference for the transmission of the GE_TXEN and GE_TXD[3:0] signals. This clock operates at 2.5 MHz, 25 MHz, or 50 MHz in MMII mode.
GE_TXD[3:0]	t/s O	LVCMOS/ LVTTL	VDD_GE	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate with bits [3:0] presented on the rising edge of GE_TXCLKOUT and bits [7:4] presented on the falling edge.
				MII Transmit Data Contains the transmit data nibble outputs that are synchronous to the GE_TXCLK input.
				GMII Transmit Data Contains the transmit data nibble outputs.
GE_TXD[7:4]	t/s O	LVCMOS/ LVTTL	VDDO	GMII Transmit Data Contains the transmit data nibble outputs. **NOTE:** Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
GE_TXCTL/GE_ TXEN	t/s O	LVCMOS/ LVTTL	VDD_GE	RGMII Transmit Control Transmit control synchronous to the GE_TXCLKOUT output rising/falling edge. GE_TXEN is presented on the rising edge of GE_TXCLKOUT. A logical derivative of GE_TXEN and GE_TxER is presented on the falling edge of GE_TXCLKOUT.
				MII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE_TXCLK.
				GMII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE_TXCLKOUT.

Table 6: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE_TXERR	t/s O	LVCMOS/ LVTTL	VDDO	MII Transmit Error It is synchronous to GE_TXCLK. **NOTE:** Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
				GMII Transmit Error It Is synchronous to GE_TXCLKOUT. **NOTE:** Multiplexed on MPP.
GE_CRS	I	LVCMOS/ LVTTL	VDDO	MII Carrier Sense Indicates that the receive medium is non-idle. In half-duplex mode, GE_CRS is also asserted during transmission. GE_CRS is not synchronous to any clock. **NOTE:** Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
				GMII Carrier Sense **NOTE:** Multiplexed on MPP.
GE_RXD[3:0]	I	LVCMOS/ LVTTL	VDD_GE	RGMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input rising/falling edge.
				MII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input.
				GMII Receive Data Contains the receive data nibble inputs.
GE_RXD[7:4]	I	LVCMOS/ LVTTL	VDDO	GMII Receive Data Contains the receive data nibble inputs. **NOTE:** Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
GE_RXERR	I	LVCMOS/ LVTTL	VDDO	MII Receive Error Indicates that an error symbol, a false carrier, or a carrier extension symbol is detected on the cable. It is synchronous to GE_RXCLK input. **NOTE:** Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
				GMII Receive Error **NOTE:** Multiplexed on MPP.

Table 6: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE_RXCTL/GE_RXDV	I	LVCMOS/LVTTL	VDD_GE	RGMII Receive Control GE_RXCTL is presented on the rising edge of GE_RXCLK. A logical derivative of GE_RXDV and GE_RXERR is presented on the falling edge of RXCLK.
				MII Receive Data Valid Indicates that valid data is present on the GE_RXD lines. It is synchronous to GE_RXCLK.
				GMII Receive Data Valid.
GE_RXCLK	I	LVCMOS/LVTTL	VDD_GE	RGMII Receive Clock The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
				MII Receive Clock Provides the timing reference for the reception of the GE_RXDV, GE_RXERR, and GE_RXD[3:0] signals. This clock operates at 2.5 MHz, 25 MHz, or 50 MHz in MMII mode.
				GMII Receive Clock Provides the timing reference for the reception of the GE_RXDV, GE_RXERR, and GE_RXD[7:0] signals. This clock operates at 125 MHz
GE_COL	I	LVCMOS/LVTTL	VDDO	MII Collision Detect Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. GE_COL is not synchronous to any clock. **NOTE:** If not using the MII interface, this pin must be left unconnected. Multiplexed on MPP (see Section 3.2, Device Pins Multiplexing, on page 41).
				GMII Collision Detect **NOTE:** Multiplexed on MPP.
GE_CLK_125	I	LVCMOS/LVTTL	VDD_GE	RGMII Clock Transmit Reference clock of 125 MHz that is used to generate GE_TXCLKOUT of 125 MHz, 25 MHz or 2.5 MHz.
				GMII Clock.
GE_MDC	t/s O	LVCMOS/LVTTL	VDD_GE	Management Data Clock MDC is the CLK input divided by 64. Provides the timing reference for the transfer of the MDIO signal.
GE_MDIO	t/s I/O	LVCMOS/LVTTL	VDD_GE	Management Data In/Out Used to transfer control information and status between PHY devices and the GbE controller. **NOTE:** When working with the SMI interface, connect the MDIO signal to a pull up resistor
VDD_GE	I	Power		Ethernet Port Gigabit Ethernet Controller Interface I/O Supply Voltage

Note The following pins are multiplexed on MPP pins: GE_TXD[7:4], GE_RXD[7:4], GE_TXERR, GE_RXERR, GE_CRS, GE_COL.

1.2.5 USB 2.0 Interface Pin Assignments

Table 7: USB 2.0 Interface Pin Assignments

Pin Name	I/O /	Pin Type	Power Rail	Description
USB_DP, USB_DM	I/O	CML	USB_AVDD	USB 2.0 port data+ and data- pair
USB_REF_CLK	I	LVTTL	VDDO	USB 2.0 port reference clock. 25 MHz.
USB_TP	O	Analog	USB_AVDD	Analog Test Point
USB_ISET	O	Analog	USB_AVDD	Current Reference Tie to VSS through a 6.04 kilohm (1%) resistor.
VBUS				This pin is not connected.
USB_AVDD	I	Power		USB 2.0 PHY quiet power supply

1.2.6 TWSI Interface Pin Assignment

Table 8: TWSI Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
TW_SDA	o/d I/O	LVTTL	VDDO	TWSI port SDA Address or write data driven by the TWSI master or read response data driven by the TWSI slave.
TW_SCK	o/d I/O	LVTTL	VDDO	TWSI port Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave.

Note When working with the TWSI interface, the TW_SDA and TW_SCK pins must be pulled up to VDDO.

1.2.7 MPP Interface Pin Assignment

Table 9: MPP Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
MPP[19:0]	t/s I/O	LVTTL	VDDO	Multi Purpose Pin Various functionalities

Note The UART1 port pins are multiplexed on MPP[19:16].

1.2.8 UART Interface Pin Assignment

Table 10: UART0 Interface

Pin Name	I/O	Pin Type	Power Rail	Description
UA0_RXD	I	LVTTL	VDDO	RX Data
UA0_TXD	O	LVTTL	VDDO	TX Data
UA0_CTSn	I	LVTTL	VDDO	Clear To Send **NOTE:** When not in use, must be pulled down to GND.
UA0_RTSn	O	LVTTL	VDDO	Ready To Send

1.2.9 Device Bus Interface Pin Assignments

Table 11: Device Bus Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
DEV_CEn[2:0]	O	LVTTL	VDDO	Device Bus Chip Enable corresponds to Bank [2:0]
DEV_BootCEn	O	LVTTL	VDDO	Device Bus Boot Chip Enable corresponds to Boot Bank
DEV_OEn	O	LVTTL	VDDO	Device Bus Output Enable **NOTE:** DEV_A[15] is multiplexed on DEV_OEn. For additional information, refer to the User Manual.
DEV_WEn[3:0]	O	LVTTL	VDDO	Device Bus Byte Write Enable **NOTE:** DEV_A[16] is multiplexed on DEV_WEn[0]. For additional information, refer to the User Manual.
DEV_ALE[1:0]	O	LVTTL	VDDO	Device Bus Address Latch Enable.
DEV_D[7:0]	t/s I/O	LVTTL	VDDO	Device Bus Multiplexed Address/Data bus **NOTE:** DEV_A[13:6] and DEV_A[26:19] are multiplexed on DEV_D[7:0]. For additional information, refer to the User Manual.
DEV_D[31:8]	t/s I/O	LVTTL	VDDO	Device Bus Data bus **NOTE:** Pins DEV_A[14] and DEV_A[15] are multiplexed on DEV_D[8]. For additional information, refer to the User Manual.
DEV_A[2:0]	t/s I/O	LVTTL	VDDO	Device Bus Address bus **NOTE:** DEV_A[5:3] and DEV_A[18:16] are multiplexed on DEV_A[2:0]. For additional information, refer to the User Manual.
DEV_READYn	I	LVTTL	VDDO	Device READY **NOTE:** When not in use, must be pulled down to GND.
DEV_BURSTn/ DEV_LASTn	O	LVTTL	VDDO	Device Burst/Device Last
TCLK_OUT	O	LVTTL	VDDO	Core Clock Output 166 MHz Device bus clock.

Note

GPP[31:16] are multiplexed on DEV_D[31:16].

1.2.10 JTAG Interface Pin Assignment

Table 12: JTAG Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
JT_CLK	I	PCI	VDDO	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_RSTn	I	PCI	VDDO	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to VSS.[1]
JT_TMS_ARM	I	PCI	VDDO	CPU JTAG Mode Select Controls the CPU JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TMS_CORE	I	PCI	VDDO	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	PCI	VDDO	JTAG Data Out Driven on the falling edge of JT_CLK.
JT_TDI	I	PCI	VDDO	JTAG Data In JTAG serial data input. Sampled with the JT_CLK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles.

Note All JTAG pads are 5V tolerant when PCI_VIO is conncted to 5V.

1.2.11 Miscellaneous Pin Assignment

The Miscellaneous signal list contains clock, reset and VDD/VSS related signals.

Table 13: Miscellaneous Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
CORE_REF_CLK	I	LVTTL	VDDO	Core Clock (TCLK) Reference Clock 25 MHz Reference clock for TCLK PLL. **NOTE:** Core Clock (TCLK) provides the clock to the internal Mbus interface, to the Device bus interface and to the MPP interface.
CPU_REF_CLK	I	LVTTL	VDDO	CPU Reference Clock 25 MHz Reference clock for CPU PLL. **NOTE:** CPU_REF_CLK provides the clock to the Feroceon CPU, local bus, MBUSL-to-MBUS bridge, and the SDRAM controller.
S_AVDD	I	Power		SysCLK PLL quiet power supply
S_AVSS	I	GND		SysCLK PLL quiet VSS
T_AVDD	I	Power		TCLK PLL quiet power supply
T_AVSS	I	GND		TCLK PLL quiet VSS
SYSRSTn	I	LVTTL	VDDO	System Reset Main reset signal of the device. Used to reset all units to their initial state. When in the reset state, most output pins are tri-stated. See Section 5.1, Hardware Reset, on page 44 for more information.
SYSRST_OUTn	o/d O	LVTTL	VDDO	Reset request indication from the device to external reset hardware. Open drain output, which is pulled-up by the internal pull-up in the 88F5281. This configuration allows connecting the signal without having to add additional logic to the hardware reset module on the board.

1.3 Internal Pull-up and Pull-down Pins List

Some pins of the device are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 150 kilohms. An external resistor with a lower value can override this internal resistor.

The internal pull-up or pull-down status for each relevant pin is listed in Table 14.

Table 14: Internal Pull-up and Pull-down Pins List

Pin Name	Pin #	Pull-up/ Pull-down
SYSRST_OUTn	W2	Pull-up
JT_TMS_ARM	U3	Pull-up
JT_RSTn	U4	Pull-down
JT_CLK	U1	Pull-down
JT_TMS_CORE	V4	Pull-up
JT_TDI	V3	Pull-up
DEV_A[0]	H20	Pull-down
DEV_A[1]	H19	Pull-down
DEV_A{2}	H18	Pull-down
DEV_D[0]	G22	Pull-down
DEV_D[1]	G21	Pull-down
DEV_D[2]	G19	Pull-up
DEV_D[3]	G18	Pull-up
DEV_D[4]	F22	Pull-up
DEV_D[5]	F21	Pull-up
DEV_D[6]	F20	Pull-down
DEV_D[7]	F19	Pull-up
DEV_D[8]	F18	Pull-up
DEV_D[9]	N20	Pull-up
DEV_D[10]	N21	Pull-up
DEV_D[11]	N22	Pull-down
DEV_D[12]	M18	Pull-down
DEV_D[13]	M19	Pull-up
DEV_D[14]	M20	Pull-up
DEV_D[15]	M21	Pull-down
DEV_D[16]	M22	Pull-down
DEV_D[17}	L22	Pull-down
DEV_D[18]	L21	Pull-up
DEV_ALE[0]	E22	Pull-down
DEV_ALE[1]	E21	Pull-down
DEV_D[19]	L19	Pull-down
DEV_D[20]	L18	Pull-down
DEV_D[21]	K22	Pull-up
DEV_D[22]	K21	Pull-down
DEV_D[23]	K20	Pull-down
DEV_D[24]	K19	Pull-down
DEV_D[25]	K18	Pull-down
DEV_D[26]	J22	Pull-down
DEV_D[27]	J21	Pull-down
DEV_D[28]	J20	Pull-down
DEV_D[29]	J19	Pull-down

2 88F5281 Pinout Map and Table

This section provides the pin map and pinout table with pin assignments for the 88F5281 device.

Due to the large number of pins, the 88F5281 pin map drawings are shown on the facing pages that follow.

Figure 2: 88F5281 Pinout Map (Top View Left Side)

	1	2	3	4	5	6	7	8	9	10	11
A	M_DQ[0]	M_DQ[1]	M_DQS[0]	M_DQ[7]	M_DQ[3]	M_CLKOUTn[0]	M_CLKOUTn[1]	M_A[11]	M_A[6]	M_A[1]	M_A[10]
B	M_DQ[5]	VSS	M_DM[0]	M_DQ[6]	M_DQ[2]	M_CLKOUT[0]	M_CLKOUT[1]	M_A[12]	M_A[8]	M_A[3]	M_BA[1]
C	M_DQ[4]	M_DQ[13]	VSS	M_DM[1]	VSS	M_DQ[10]	M_STARTBURST	VSS	M_A[7]	M_A[4]	VSS
D	M_CAL	M_DQ[12]	M_DQ[8]	M_DQ[9]	M_DQS[1]	M_DQ[15]	M_STARTBURST_IN	M_CKE[1]	M_A[9]	M_A[5]	M_A[0]
E	UA0_CTSn	UA0_TXD	UA0_RTSn	UA0_RXD	VSS	M_DQ[14]	M_DQ[11]	M_CKE[0]	VSS	M_SSTL_VREF	M_A[2]
F	MPP[18]	MPP[17]	NC	MPP[19]	MPP[16]			VDD_CPU			VDD_CPU
G	CPU_REF_CLK	VSS	CORE_REF_CLK	VSS	USB_REF_CLK		VDD_CPU	VDD_M	VDD_CPU	VDD_CPU	VDD_CPU
H	GE_CLK_125	GE_MDIO	VSS	GE_MDC	VSS		VDD_CPU	VDD_CPU	VDD_M	VDD_M	VDD_M
J	GE_TXCTL	GE_TXD[0]	GE_TXD[1]	GE_TXD[2]	GE_TXD[3]		VDD_CPU	VDD_M	VSS	VSS	VSS
K	GE_RXCTL	GE_RXD[0]	GE_RXCLK	GE_TXCLK	GE_TXCLKOUT		VDD_CPU	S_AVDD	VDDO	VSS	VSS
L	GE_RXD[3]	GE_RXD[1]	VSS	GE_RXD[2]	VSS			S_AVSS	VDD_GE	VSS	VDD_CORE
M	MPP[11]	MPP[12]	MPP[13]	MPP[14]	MPP[15]			VDDO	VDD_GE	VSS	VSS
N	MPP[8]	VSS	MPP[9]	MPP[10]	T_AVDD			VDD_CORE	VSS	VSS	VDD_CORE
P	USB_DM	USB_DP	USB_TP	VBUS	T_AVSS			USB_AVDD	VSS	VSS	VSS
R	MPP[2]	VSS	MPP[1]	MPP[0]	USB_ISET			VDDO	VDDO	VSS	VSS
T	MPP[6]	MPP[5]	MPP[4]	MPP[3]	VSS			PCI_AVSS	PCI_AVDD	VDDO	VDDO
U	JT_CLK	JT_TDO	JT_TMS_ARM	JT_RSTn	MPP[7]						
V	PCI_HS	PCI_ENUMn	JT_TDI	JT_TMS_CORE	VSS	PCI_PAD[26]	PCI_PAD[22]	PCI_PAD[18]	VSS	PCI_PAR	PCI_PAD[13]
W	PCI_LED	SYSRST_OUTn	PCI_INTn	SYSRSTn	PCI_PAD[30]	PCI_PAD[24]	PCI_PAD[20]	PCI_PAD[16]	PCI_TRDYn	PCI_PAD[15]	PCI_PAD[11]
Y	PCI_VIO	PCI_CAL	VSS	PCI_GNTn	PCI_PAD[28]	PCI_IDSEL	VSS	PCI_FRAMEn	PCI_STOPn	VSS	PCI_PAD[9]
AA	PCI_CLK	VSS	PCI_PAD[29]	PCI_PAD[25]	PCI_PAD[23]	PCI_PAD[19]	PCI_CBEn[2]	PCI_DEVSELn	PCI_SERRn	PCI_PAD[14]	PCI_PAD[10]
AB	PCI_REQn	PCI_PAD[31]	PCI_PAD[27]	PCI_CBEn[3]	PCI_PAD[21]	PCI_PAD[17]	PCI_IRDYn	PCI_PERRn	PCI_CBEn[1]	PCI_PAD[12]	PCI_M66EN
	1	2	3	4	5	6	7	8	9	10	11

Figure 3: 88F5281 Pinout Map (Top View Right Side)

12	13	14	15	16	17	18	19	20	21	22	
M_CSn[0]	M_WEn	M_CSn[1]	M_ODT[2]	M_DQ[16]	M_DM[2]	M_DQ[22]	M_DQ[18]	DEV_BURSTn	DEV_READYn	DEV_BootCEn	A
M_CSn[2]	M_CASn	M_CSn[3]	M_DQ[20]	M_DQ[17]	M_DQS[2]	M_DQ[23]	M_DQ[19]	TCLK_OUT	NC	DEV_OEn	B
M_RASn	M_ODT[1]	VSS	M_DQ[21]	M_DQ[24]	VSS	M_DQ[31]	M_DQ[27]	VSS	DEV_CEn[2]	DEV_CEn[1]	C
M_BA[0]	M_ODT[3]	M_ODT[0]	M_DQ[28]	M_DQ[25]	M_DQS[3]	M_DQ[26]	P_CAL	DEV_CEn[0]	DEV_WEn[3]	DEV_WEn[2]	D
VSS	M_A[13]	VSS	M_DQ[29]	M_DM[3]	M_DQ[30]	VSS	DEV_WEn[1]	DEV_WEn[0]	DEV_ALE[1]	DEV_ALE[0]	E
						DEV_D[8]	DEV_D[7]	DEV_D[6]	DEV_D[5]	DEV_D[4]	F
VDD_CPU	VDD_CORE	VDD_M	VDD_M			DEV_D[3]	DEV_D[2]	VSS	DEV_D[1]	DEV_D[0]	G
VDD_M	VDD_M	VDD_M	VDDO			DEV_A[2]	DEV_A[1]	DEV_A[0]	DEV_D[31]	DEV_D[30]	H
VSS	VSS	VSS	VDDO			VSS	DEV_D[29]	DEV_D[28]	DEV_D[27]	DEV_D[26]	J
VSS	VSS	VSS	VDDO			DEV_D[25]	DEV_D[24]	DEV_D[23]	DEV_D[22]	DEV_D[21]	K
VDD_CORE	VSS	VSS	VDD_CORE			DEV_D[20]	DEV_D[19]	VSS	DEV_D[18]	DEV_D[17]	L
VSS	VSS	PEX_AVDD	PEX_AVDT			DEV_D[12]	DEV_D[13]	DEV_D[14]	DEV_D[15]	DEV_D[16]	M
VDD_CORE	VSS	VSS	PEX_AVDL			VDD_CPU	VSS	DEV_D[9]	DEV_D[10]	DEV_D[11]	N
VSS	VSS	VSS	VDDO			PEX_HSDACN	PEX_CLKn	VSS	PEX_ISET	VSS	P
VDD_CPU	VSS	VSS	VDDO			PEX_HSDACP	PEX_CLKp	VSS	PEX_Tn	PEX_Rn	R
VDD_CORE	VDDO	VDDO	VDDO			VSS	VSS	VSS	PEX_T	PEX_R	T
						PCI_PAD[32]	TW_SCK	TW_SDA	PEX_TP	VSS	U
VSS	PCI_PAD[2]	VSS	PCI_PAR64	PCI_PAD[60]	VSS	PCI_PAD[50]	PCI_PAD[46]	PCI_PAD[38]	PCI_PAD[36]	PCI_PAD[34]	V
PCI_PAD[6]	PCI_PAD[4]	PCI_REQ64n	PCI_CBEn[5]	PCI_PAD[62]	PCI_PAD[56]	PCI_PAD[52]	VSS	PCI_PAD[42]	PCI_PAD[40]	PCI_PAD[33]	W
PCI_CBEn[0]	VSS	PCI_PAD[0]	PCI_CBEn[7]	VSS	PCI_PAD[58]	PCI_PAD[54]	PCI_PAD[48]	PCI_PAD[44]	PCI_PAD[35]	PCI_PAD[37]	Y
PCI_PAD[7]	PCI_PAD[3]	PCI_ACK64n	PCI_CBEn[4]	PCI_PAD[61]	PCI_PAD[57]	PCI_PAD[53]	PCI_PAD[49]	PCI_PAD[45]	VSS	PCI_PAD[39]	AA
PCI_PAD[8]	PCI_PAD[5]	PCI_PAD[1]	PCI_CBEn[6]	PCI_PAD[63]	PCI_PAD[59]	PCI_PAD[55]	PCI_PAD[51]	PCI_PAD[47]	PCI_PAD[43]	PCI_PAD[41]	AB
12	13	14	15	16	17	18	19	20	21	22	

Table 15: 88F5281 Pin List

Ball	Pin	Ball	Pin	Ball	Pin	Ball	Pin
A01	M_DQ[0]	C03	VSS	E05	VSS	G20	VSS
A02	M_DQ[1]	C04	M_DM[1]	E06	M_DQ[14]	G21	DEV_D[1]
A03	M_DQS[0]	C05	VSS	E07	M_DQ[11]	G22	DEV_D[0]
A04	M_DQ[7]	C06	M_DQ[10]	E08	M_CKE[0]	H01	GE_CLK_125
A05	M_DQ[3]	C07	M_STARTBURST	E09	VSS	H02	GE_MDIO
A06	M_CLKOUTn[0]	C08	VSS	E10	M_SSTL_VREF	H03	VSS
A07	M_CLKOUTn[1]	C09	M_A[7]	E11	M_A[2]	H04	GE_MDC
A08	M_A[11]	C10	M_A[4]	E12	VSS	H05	VSS
A09	M_A[6]	C11	VSS	E13	M_A[13]	H07	VDD_CPU
A10	M_A[1]	C12	M_RASn	E14	VSS	H08	VDD_CPU
A11	M_A[10]	C13	M_ODT[1]	E15	M_DQ[29]	H09	VDD_M
A12	M_CSn[0]	C14	VSS	E16	M_DM[3]	H10	VDD_M
A13	M_WEn	C15	M_DQ[21]	E17	M_DQ[30]	H11	VDD_M
A14	M_CSn[1]	C16	M_DQ[24]	E18	VSS	H12	VDD_M
A15	M_ODT[2]	C17	VSS	E19	DEV_WEn[1]	H13	VDD_M
A16	M_DQ[16]	C18	M_DQ[31]	E20	DEV_WEn[0]	H14	VDD_M
A17	M_DM[2]	C19	M_DQ[27]	E21	DEV_ALE[1]	H15	VDDO
A18	M_DQ[22]	C20	VSS	E22	DEV_ALE[0]	H18	DEV_A[2]
A19	M_DQ[18]	C21	DEV_CEn[2]	F01	MPP[18]	H19	DEV_A[1]
A20	DEV_BURSTn	C22	DEV_CEn[1]	F02	MPP[17]	H20	DEV_A[0]
A21	DEV_READYn	D01	M_CAL	F03	NC	H21	DEV_D[31]
A22	DEV_BootCEn	D02	M_DQ[12]	F04	MPP[19]	H22	DEV_D[30]
B01	M_DQ[5]	D03	M_DQ[8]	F05	MPP[16]	J01	GE_TXCTL
B02	VSS	D04	M_DQ[9]	F08	VDD_CPU	J02	GE_TXD[0]
B03	M_DM[0]	D05	M_DQS[1]	F11	VDD_CPU	J03	GE_TXD[1]
B04	M_DQ[6]	D06	M_DQ[15]	F18	DEV_D[8]	J04	GE_TXD[2]
B05	M_DQ[2]	D07	M_STARTBURST_IN	F19	DEV_D[7]	J05	GE_TXD[3]
B06	M_CLKOUT[0]	D08	M_CKE[1]	F20	DEV_D[6]	J07	VDD_CPU
B07	M_CLKOUT[1]	D09	M_A[9]	F21	DEV_D[5]	J08	VDD_M
B08	M_A[12]	D10	M_A[5]	F22	DEV_D[4]	J09	VSS
B09	M_A[8]	D11	M_A[0]	G01	CPU_REF_CLK	J10	VSS
B10	M_A[3]	D12	M_BA[0]	G02	VSS	J11	VSS
B11	M_BA[1]	D13	M_ODT[3]	G03	CORE_REF_CLK	J12	VSS
B12	M_CSn[2]	D14	M_ODT[0]	G04	VSS	J13	VSS
B13	M_CASn	D15	M_DQ[28]	G05	USB_REF_CLK	J14	VSS
B14	M_CSn[3]	D16	M_DQ[25]	G07	VDD_CPU	J15	VDDO
B15	M_DQ[20]	D17	M_DQS[3]	G08	VDD_M	J18	VSS
B16	M_DQ[17]	D18	M_DQ[26]	G09	VDD_CPU	J19	DEV_D[29]
B17	M_DQS[2]	D19	P_CAL	G10	VDD_CPU	J20	DEV_D[28]
B18	M_DQ[23]	D20	DEV_CEn[0]	G11	VDD_CPU	J21	DEV_D[27]
B19	M_DQ[19]	D21	DEV_WEn[3]	G12	VDD_CPU	J22	DEV_D[26]
B20	TCLK_OUT	D22	DEV_WEn[2]	G13	VDD_CORE	K01	GE_RXCTL
B21	NC	E01	UA0_CTSn	G14	VDD_M	K02	GE_RXD[0]
B22	DEV_OEn	E02	UA0_TXD	G15	VDD_M	K03	GE_RXCLK
C01	M_DQ[4]	E03	UA0_RTSn	G18	DEV_D[3]	K04	GE_TXCLK
C02	M_DQ[13]	E04	UA0_RXD	G19	DEV_D[2]	K05	GE_TXCLKOUT

Table 15: 88F5281 Pin List (Continued)

Ball	Pin	Ball	Pin	Ball	Pin
K07	VDD_CPU	M19	DEV_D[13]	R09	VDDO
K08	S_AVDD	M20	DEV_D[14]	R10	VSS
K09	VDDO	M21	DEV_D[15]	R11	VSS
K10	VSS	M22	DEV_D[16]	R12	VDD_CPU
K11	VSS	N01	MPP[8]	R13	VSS
K12	VSS	N02	VSS	R14	VSS
K13	VSS	N03	MPP[9]	R15	VDDO
K14	VSS	N04	MPP[10]	R18	PEX_HSDACP
K15	VDDO	N05	T_AVDD	R19	PEX_CLKp
K18	DEV_D[25]	N08	VDD_CORE	R20	VSS
K19	DEV_D[24]	N09	VSS	R21	PEX_Tn
K20	DEV_D[23]	N10	VSS	R22	PEX_Rn
K21	DEV_D[22]	N11	VDD_CORE	T01	MPP[6]
K22	DEV_D[21]	N12	VDD_CORE	T02	MPP[5]
L01	GE_RXD[3]	N13	VSS	T03	MPP[4]
L02	GE_RXD[1]	N14	VSS	T04	MPP[3]
L03	VSS	N15	PEX_AVDDL	T05	VSS
L04	GE_RXD[2]	N18	VDD_CPU	T08	PCI_AVSS
L05	VSS	N19	VSS	T09	PCI_AVDD
L08	S_AVSS	N20	DEV_D[9]	T10	VDDO
L09	VDD_GE	N21	DEV_D[10]	T11	VDDO
L10	VSS	N22	DEV_D[11]	T12	VDD_CORE
L11	VDD_CORE	P01	USB_DM	T13	VDDO
L12	VDD_CORE	P02	USB_DP	T14	VDDO
L13	VSS	P03	USB_TP	T15	VDDO
L14	VSS	P04	VBUS	T18	VSS
L15	VDD_CORE	P05	T_AVSS	T19	VSS
L18	DEV_D[20]	P08	USB_AVDD	T20	VSS
L19	DEV_D[19]	P09	VSS	T21	PEX_T
L20	VSS	P10	VSS	T22	PEX_R
L21	DEV_D[18]	P11	VSS	U01	JT_CLK
L22	DEV_D[17]	P12	VSS	U02	JT_TDO
M01	MPP[11]	P13	VSS	U03	JT_TMS_ARM
M02	MPP[12]	P14	VSS	U04	JT_RSTn
M03	MPP[13]	P15	VDDO	U05	MPP[7]
M04	MPP[14]	P18	PEX_HSDACN	U18	PCI_PAD[32]
M05	MPP[15]	P19	PEX_CLKn	U19	TW_SCK
M08	VDDO	P20	VSS	U20	TW_SDA
M09	VDD_GE	P21	PEX_ISET	U21	PEX_TP
M10	VSS	P22	VSS	U22	VSS
M11	VSS	R01	MPP[2]	V01	PCI_HS
M12	VSS	R02	VSS	V02	PCI_ENUMn
M13	VSS	R03	MPP[1]	V03	JT_TDI
M14	PEX_AVDD	R04	MPP[0]	V04	JT_TMS_CORE
M15	PEX_AVDDT	R05	USB_ISET	V05	VSS
M18	DEV_D[12]	R08	VDDO	V06	PCI_PAD[26]

Table 15: 88F5281 Pin List (Continued)

Ball	Pin	Ball	Pin	Ball	Pin
V07	PCI_PAD[22]	Y09	PCI_STOPn	AB11	PCI_M66EN
V08	PCI_PAD[18]	Y10	VSS	AB12	PCI_PAD[8]
V09	VSS	Y11	PCI_PAD[9]	AB13	PCI_PAD[5]
V10	PCI_PAR	Y12	PCI_CBEn[0]	AB14	PCI_PAD[1]
V11	PCI_PAD[13]	Y13	VSS	AB15	PCI_CBEn[6]
V12	VSS	Y14	PCI_PAD[0]	AB16	PCI_PAD[63]
V13	PCI_PAD[2]	Y15	PCI_CBEn[7]	AB17	PCI_PAD[59]
V14	VSS	Y16	VSS	AB18	PCI_PAD[55]
V15	PCI_PAR64	Y17	PCI_PAD[58]	AB19	PCI_PAD[51]
V16	PCI_PAD[60]	Y18	PCI_PAD[54]	AB20	PCI_PAD[47]
V17	VSS	Y19	PCI_PAD[48]	AB21	PCI_PAD[43]
V18	PCI_PAD[50]	Y20	PCI_PAD[44]	AB22	PCI_PAD[41]
V19	PCI_PAD[46]	Y21	PCI_PAD[35]		
V20	PCI_PAD[38]	Y22	PCI_PAD[37]		
V21	PCI_PAD[36]	AA01	PCI_CLK		
V22	PCI_PAD[34]	AA02	VSS		
W01	PCI_LED	AA03	PCI_PAD[29]		
W02	SYSRST_OUTn	AA04	PCI_PAD[25]		
W03	PCI_INTn	AA05	PCI_PAD[23]		
W04	SYSRSTn	AA06	PCI_PAD[19]		
W05	PCI_PAD[30]	AA07	PCI_CBEn[2]		
W06	PCI_PAD[24]	AA08	PCI_DEVSELn		
W07	PCI_PAD[20]	AA09	PCI_SERRn		
W08	PCI_PAD[16]	AA10	PCI_PAD[14]		
W09	PCI_TRDYn	AA11	PCI_PAD[10]		
W10	PCI_PAD[15]	AA12	PCI_PAD[7]		
W11	PCI_PAD[11]	AA13	PCI_PAD[3]		
W12	PCI_PAD[6]	AA14	PCI_ACK64n		
W13	PCI_PAD[4]	AA15	PCI_CBEn[4]		
W14	PCI_REQ64n	AA16	PCI_PAD[61]		
W15	PCI_CBEn[5]	AA17	PCI_PAD[57]		
W16	PCI_PAD[62]	AA18	PCI_PAD[53]		
W17	PCI_PAD[56]	AA19	PCI_PAD[49]		
W18	PCI_PAD[52]	AA20	PCI_PAD[45]		
W19	VSS	AA21	VSS		
W20	PCI_PAD[42]	AA22	PCI_PAD[39]		
W21	PCI_PAD[40]	AB01	PCI_REQn		
W22	PCI_PAD[33]	AB02	PCI_PAD[31]		
Y01	PCI_VIO	AB03	PCI_PAD[27]		
Y02	PCI_CAL	AB04	PCI_CBEn[3]		
Y03	VSS	AB05	PCI_PAD[21]		
Y04	PCI_GNTn	AB06	PCI_PAD[17]		
Y05	PCI_PAD[28]	AB07	PCI_IRDYn		
Y06	PCI_IDSEL	AB08	PCI_PERRn		
Y07	VSS	AB09	PCI_CBEn[1]		
Y08	PCI_FRAMEn	AB10	PCI_PAD[12]		

Table 15: 88F5281 Pin List (Continued)

3 Pin Multiplexing

3.1 MPP Multiplexing

The 88F5281 device contains 20 Multi Purpose Pins (MPP). Each one can be assigned to a different functionality through the MPP Control register.

- GPIO: General Purpose In/Out Port, see the General Purpose I/O Port section in the *88F5281 User Manual.*
- PCI_REQn[5:2]/PCI_GNTn[5:2]: PCI Arbitration Signals, see the PCI Interface section in the *88F5281 User Manual.* PCI_PMEn: PCI Power Management Event, see the PCI interface section in the 88F5281 *Datasheet User Manual.*
- GE_TXD[7:4]/GE_RXD[7:4]: GbE port Signals when configured to GMII interface. see the Gigabit Ethernet Controller section in the 88F5281 Datasheet User Manual.
- GE_TXER, GE_RXER, GE_CRS, GE_COL: GbE port Signals when configured to GMII or MII interface.
- PEX_RST_OUTn - optional PCI Express boards reset output.
- UA1_RXD, UA1_TXD, UA1_CTSn, UA1_RTSn - UART1 pins.

Table 16 shows each MPP pins' functionality as determined by the MPP Multiplex register, see the Pins Multiplexing Interface Registers section in the *88F5281 User Manual*.

Table 16: MPP Function Summary

MPP Pin[1]	0x0	0x1	0x2	0x3	0x4
MPP[0]	PEX_RST_OUTn		PCI_REQn[2] (in)	GPIO[0] (in/out)	
MPP[1]	GPIO[1] (in/out)		PCI_GNTn[2] (out)		
MPP[2]	GPIO[2] (in/out)		PCI_REQn[3] (in)	PCI_PMEn (out)	
MPP[3]	GPIO[3] (in/out)		PCI_GNTn[3] (out)		
MPP[4]	GPIO[4] (in/out)		PCI_REQn[4] (in)		BOOT NAND Flash REn (out)
MPP[5]	GPIO[5] (in/out)		PCI_GNTn[4] (out)		BOOT NAND Flash WEn (out)
MPP[6]	GPIO[6] (in/out)		PCI_REQn[5] (in)		NAND Flash REn[0] (out)
MPP[7]	GPIO[7] (in/out)		PCI_GNTn[5] (out)		NAND Flash WEn[0] (out)
MPP[8]	GPIO[8] (in/out)	GE_COL (in)			

Table 16: MPP Function Summary (Continued)

MPP Pin[1]	0x0	0x1	0x2	0x3	0x4
MPP[9]	GPIO[9] (in/out)	GE_RXERR (in)			
MPP[10]	GPIO[10] (in/out)	GE_CRS (in)			
MPP[11]	GPIO[11] (in/out)	GE_TXERR (out)			
MPP[12]	GPIO[12] (in/out)	GE_TXD[4] (out)			NAND Flash REn[1] (out)
MPP[13]	GPIO[13] (in/out)	GE_TXD[5] (out)			NAND Flash WEn[1] (out)
MPP[14]	GPIO[14] (in/out)	GE_TXD[6] (out)			NAND Flash REn[2] (out)
MPP[15]	GPIO[15] (in/out)	GE_TXD[7] (out)			NAND Flash WEn[2] (out)
MPP[16]	UA1_RXD (in)	GE_RXD[4] (in)			
MPP[17]	UA1_TXD (out)	GE_RXD[5] (in)			
MPP[18]	UA1_CTSn (in)	GE_RXD[6] (in)			
MPP[19]	UA1_RTSn (out)	GE_RXD[7] (in)			

1. MPP[7:0] are 5V tolerant when PCI_VIO is connected to 5V.

- Depending on its configured functionality, each pin might act as output or input pin. All the MPP pins wake up after reset in 0x0 mode: MPP[0] wakes up as PEX_RST_OUTn after reset, MPP[15:1] pins wake up after reset as GPIO input pins and MPP[19:16] wake up as UART1 pins after reset.
- Pins that are left as GPIO (For MPP[15:8]) and are not connected should be set to output after SYSRST de-assertion.

3.2 Device Pins Multiplexing

When connected to 16-bit or 8-bit devices on the device interface, pins DEV_D[31:16] can be configured to act as additional GPIO pins.

Table 17 shows DEV_D[31:16] pins' functionality as determined by the Device Multiplex register, see the Pins Multiplexing Interface Registers section in the *88F5281 Datasheet User Manual*.

Table 17: DEV_D[31:16] Function Summary

MPP Pin	0x0	0x1
DEV_D[31:16]	DEV_D[31:16] (in/out)	GPIO[31:16] (in/out)

Note

Depending on its configured functionality, each pin might act as output or input pin. All DEV_D pins wake up after reset as DEV_D input pins.

3.3 Gigabit Ethernet (GbE) Pins Multiplexing on MPP

The 88F5281 has 16 dedicated pins for its GbE port. The port can be configured to have MII/GMII/RGMII interface to the external PHY or switch device. When configured to GMII, GE_TXD[7:4]/GE_RXD[7:4] pins are multiplexed on the MPP. When configured to GMII or MII GE_TXER, GE_RXER, GE_CRS, GE_COL pins are multiplexed on the MPP.

Table 18, Ethernet Port Pins Multiplexing, on page 42 summarizes the GbE port pins multiplexing.

Table 18: Ethernet Port Pins Multiplexing

Pin Name	GMII	MII	RGMII
GE_TXCLK	NA	GE_TXCLK (in)	NA
GE_TXCLKOUT	GE_TXCLKOUT (out)	NA	GE_TXCLKOUT (out)
GE_TXD[3:0]	GE_TXD[3:0] (out)	GE_TXD[3:0] (out)	GE_TXD[3:0] (out)
GE_TXEN	GE_TXEN (out)	GE_TXEN (out)	GE_TXCTL (out)
GE_RXD[3:0]	GE_RXD[3:0] (in)	GE_RXD[3:0] (in)	GE_RXD[3:0] (in)
GE_RXDV	GE_RXDV (in)	GE_RXDV (in)	GE_RXCTL (in)
GE_RXCLK	GE_RXCLK (in)	GE_RXCLK (in)	GE_RXCLK (in)
MPP[15:12]	GE_TXD[7:4] (out)	NA	NA
MPP[19:16]	GE_RXD[7:4] (in)	NA	NA
MPP[11]	GE_TXERR (out)	GE_TXERR (out)	NA
MPP[9]	GE_RXERR (in)	GE_RXERR (in)	NA
MPP	GE_CRS (out)	GE_CRS (out)	NA
MPP	GE_COL (in)	GE_COL (in)	NA
GE_CLK125	GE_CLK125 (in)	NA (in)	GE_CLK125 (in)
GE_MDC (out)	GE_MDC (out)	GE_MDC (out)	GE_MDC (out)
GE_MDIO (in/out)	GE_MDIO (in/out)	GE_MDIO (in/out)	GE_MDIO (in/out)

4 Clocking

4.1 Reference Clocks

The following table lists the clocks.

Table 19: Reference Clocks

PLL/DLL	Description
CPU PLL	■ Reference clock • CPU_REF_CLK (25 MHz) ■ Derivative clocks • CPU Clock • DDR Clock (the AHB bus uses the DDR clock).
Core PLL	■ Reference clock • CORE_REF_CLK (25 MHz) ■ Derivative clocks • TCLK
PEX PLL	■ Reference clock • PEX_CLKp, PEX_CLKn (100 MHz) differential clock ■ Derivative clocks • PEXClock
USB PLL	■ Reference clock • USB_REF_CLK (25 MHz) ■ Derivative clocks • USBCLK
PCI DLL	■ Reference clock • Clock is derived directly from PCI_CLK, running at the PCI interface frequency (133 / 100 / 66 / 33 and below MHz) ■ Derivative clocks • None

The function of each CPU/DDR Clock Frequency Ratio mode is defined in field CPU/DDR Clock Frequency Ratio after reset (see CPU/DDR Clock Frequency Ratio in Table 21, Reset Configuration, on page 47).

5 Reset Configuration

5.1 Hardware Reset

The 88F5281 has one reset input pin — SYSRSTn. When asserted, the entire chip is placed in its initial state. All outputs except some output pins are placed in high-z.

The following output pins are still active during SYSRSTn assertion:

- DEV_CEn[2:0]
- DEV_BootCEn
- TCLK_OUT
- GE_TXCLKOUT
- M_CLKOUT[1:0], M_CLKOUTn[1:0]
- M_CKE[1:0]
- M_ODT[3:0]
- M_STARTBURST
- PEX_HSDACN
- PEX_HSDACP
- PEX_ISET
- PEX_T
- PEX_Tn
- PCI_CAL
- USB_DM
- USB_DP
- USB_TP
- MPP[16:0]—may change according to reset sample setting.

The 88F5281 has an SYSRST_OUTn output signal, that is used as a reset request from the 88F5281 to the board reset logic. This signal is set when one of the following maskable events occurs:

- Received hot reset indication from the PCI Express link (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see Part 2 of 2: User Manual). In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles.
- PCI Express link failure (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register. In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles.
- Watchdog timer expiration and bit <WDRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register.

Note

Reset must be active for a minimum length of 100ms. Core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

5.2 PCI Express Reset

The PCI Express specification defines two ways to reset the PCI Express interface. In addition, Link failure condition has a similar affect to PCI Express resets.

As a root complex the 88F5281 may generate a reset to the PCI Express port in any of the following ways:

Fundamental reset	The board reset logic generates reset signal to the PERST# pin in the PCI Express connector. The board reset logic must also generate a reset signal to the SYSRSTn pin of the 88F5281. When the SYSRSTn pin is asserted, the entire chip is reset, including the PCI Express interface logic and registers.
Hot reset	Hot reset is triggered by the CPU core by setting the conf_mstr_hot_reset bit in the PCI Express Control register (see *88F5281 Feroceon® User Manual*). When Hot reset is triggered, the PCI Express interface is reset. All PCI Express interface registers, except sticky bits, are reset. A maskable interrupt is asserted.
Link fail reset	Link failure is detected when the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected, the PCI Express interface is reset. A maskable interrupt is asserted.

5.2.1 PCI Express Reset in Endpoint Mode

When working in Endpoint mode, both link fail and hot reset conditions trigger a chip internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.

As a endpoint the 88F5281 receives a reset from the PCI Express port in any of the following ways:

Fundamental reset	Fundamental reset is indicated by the assertion of PERST# pin in the PCI Express connector. The PERST# pin must be connected via the board reset logic to the SYSRSTn input pin. See "Section 5.1, Hardware Reset, on page 44" for further details. The board reset logic must also generate a reset signal to the rest or the board logic. When the SYSRSTn pin is asserted, the entire chip is reset, including the PCI Express interface logic and registers.
Hot reset	Hot reset is triggered by the reception of a Hot reset packet from the PCI Express port. When a Hot reset packet is received, the 88F5281 triggers an internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.
Link fail reset	Link failure is detected when the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected, the 88F5281 triggers an internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.

Note

When working in Endpoint mode, clear bits [16], [17], and [19] of the PCI Express register at offset 0x41A60.

The endpoint reset scheme flow appears in Figure 4, Endpoint Reset Scheme, on page 46. Table 20, Endpoint Reset Scheme, on page 46 describes each of the pins mentioned in the figure.

Figure 4: Endpoint Reset Scheme

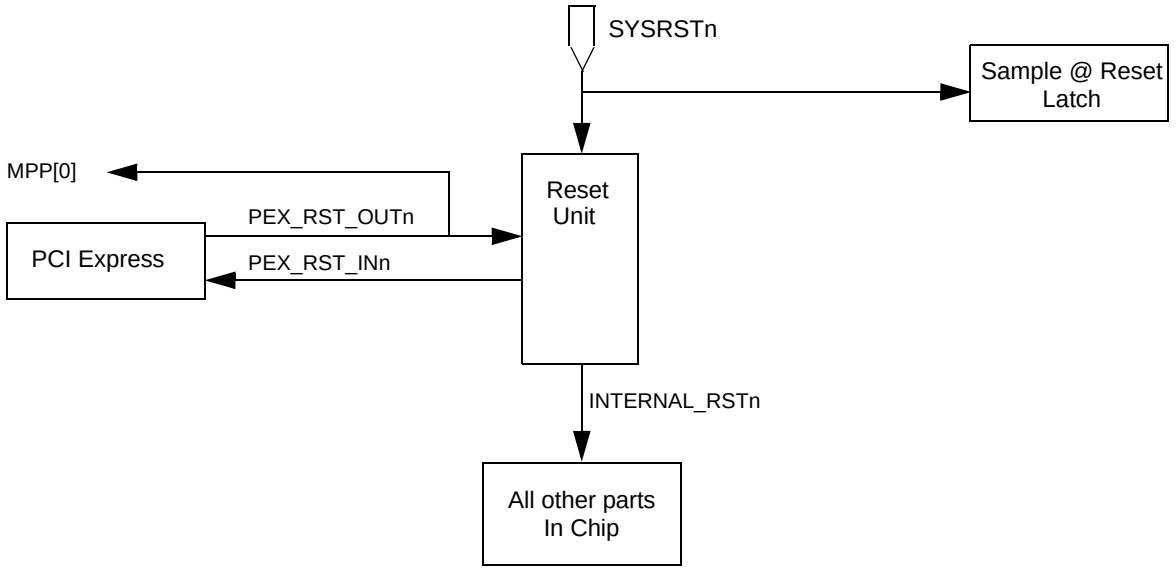


Table 20: Endpoint Reset Scheme

Signal Name	Active
MPP[0]	Active when one of the following occurs: • PEX_RST_OUTn is active.
PEX_RST_OUTn	Active when one of the following occurs: • PEX Link failure occurs and is not masked. • PEX Hot reset occurs and is not masked. **NOTE:** The mask bits are sticky and reset by SYSRSTn only
PEX_RST_INn	Active when one of the following occurs: • SYSRSTn is asserted (synchronized to TCLK).
INTERNAL_RESET	Active when one of the following occurs: • SYSRSTn is asserted (synchronized to TCLK). • PEX_RST_OUTn is asserted.

5.3 PCI/PCI-X Reset

When working as a PCI/PCI-X add-in card, the PRST# pin in the PCI/PCI-X connector should be connected to the SYSRSTn input pin. See Section 5.1, Hardware Reset, on page 44 for further details.

5.4 Feroceon CPU Tap Controller Reset

Reset when JT_RSTn is set and JT_TMS_ARM is active.

5.5 Pins Sample Configuration

The following pins are sampled during SYSRSTn de-assertion. Internal pull up/down resisters set the default mode. External pull up/down resisters are required to change the default mode of operation. These signals must remain pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).

Note

- All internal pull-up/down resistors are 150 kilohms.
- Most of the reset strapping pins integrate a weak pull-up or pull-down resistor (indicated in Table 21 as pulled up to 1 or pulled down to 0, respectively). When using latches, buffers, or other logic that can change the signal logic level (i.e., bus holders), it is highly recommended to use external resistors (for additional information, refer to the *Orion SoC Hardware Design Guide*).
- See Table 14, Internal Pull-up and Pull-down Pins List, on page 32 for the full list of integrated internal pull-up/down resistors in the device.

Table 21: Reset Configuration

Pin	Configuration Function
DEV_D[0]	Serial ROM initialization
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled down to 0.
DEV_D[1]	Watchdog enable
	0 = Watchdog Disable 1 = Watchdog Enable **NOTE:** Internally pulled down to 0.
DEV_D[3]	PCI Express mode select
	0 = Endpoint 1 = Root Complex **NOTE:** Internally pulled up to 1. When working in Endpoint mode, and expansion ROM is used; expansion ROM parameters need to be configured during the serial initialization phase.
DEV_D[5]	DRAM type
	0 = DDR1 SDRAM 1 = DDR2 SDRAM **NOTE:** Internally pulled up to 1.

Table 21: Reset Configuration (Continued)

Pin	Configuration Function
DEV_D[19], DEV_D[16], DEV_D[15], DEV_D[4], DEV_D[2]	CPU/DDR clock frequency ratio
	0 = Reserved 1 = 400/200 MHz 2 = 400/133 MHz 3 = 500/167 MHz (Internal default) 4–1F = Reserved **NOTE:** Internal default value: 0x3 (CPU 500 MHz, DDR 167 MHz). The pins are listed in MSB to LSB order.
DEV_D[7:6]	TCLK frequency
	0x0 = Reserved 0x1 = Reserved 0x2 = 166 MHz 0x3 = Reserved **NOTE:** Internally pulled to 0x2.
DEV_A[1:0], DEV_ALE[1:0]	MPP multiplex
	Define default mode for MPP multiplex. It is the same value for all of the pins. See Table 16: "MPP Function Summary", on page 39. **NOTE:** Internally pulled to 0x0. Mode[3:0] = DEV_A[1:0], DEV_ALE[1:0]. The pins are listed in MSB to LSB order.
DEV_A[2]	Reserved
	Reserved Must be sampled at 0. **NOTE:** Internally pulled down to 0.
DEV_D[10:8]	Gigabit Ethernet Port Mode select
	000 = Unused 001 = Reserved 010 = GMII 011 = MII 100 = Reserved 101 = Reserved 110 = Reserved 111 = RGMII (default) **NOTE:** Internally pulled up to 111.
DEV_D[12:11]	DEV_BootCEn device width
	00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = Reserved **NOTE:** Internally pulled down to 00.

Table 21: Reset Configuration (Continued)

Pin	Configuration Function
DEV_D[17]	Big Endian initialization
	0 = Little Endian 1 = Big Endian **NOTE:** Internally pulled down to 0.
DEV_D[18]	Reserved for future use.
	Reserved Must be sampled at 1. **NOTE:** Internally pull up to 1.
DEV_D[20]	Reserved for future use.
	Reserved Must be sampled at 0. **NOTE:** Internally pulled down to 0.
DEV_D[21]	Reserved for future use.
	Reserved Must be sampled at 1. **NOTE:** Internally pull up to 1.
DEV_D[24:22]	Reserved for future use.
	Reserved Must be sampled at 0. **NOTE:** Internally pulled down to 0.
DEV_D[25]	Boot from NAND Flash
	Defines the default value of bit <NFBoot> in the NAND Flash Control Register (see the *88F5281 User Manual*) 0 = Boot not from NAND Flash 1 = Boot from NAND Flash • When DEV_D[25] and DEV_D[26] are both set to 1, fields <MPPSel4> and <MPPSel5> in the MPP Control 0 Register are set to 0x4 (see the *88F5281 User Manual*). These fields are cleared to 0x0 otherwise. **NOTE:** Internally pulled down to 0.
DEV_D[26]	Boot from CE care NAND Flash
	Defines the default value of bit <NFActCEnBoot> in the NAND Flash Control Register (see the *88F5281 User Manual*) 0 = Boot from CE don't care NAND Flash 1 = Boot from CE care NAND Flash • When DEV_D[25] and DEV_D[26] are both set to 1, fields <MPPSel4> and <MPPSel5> in the MPP Control 0 Register are set to 0x4 (see the *88F5281 User Manual*). These fields are cleared to 0x0 otherwise. **NOTE:** Internally pulled down to 0.

Table 21: Reset Configuration (Continued)

Pin	Configuration Function
DEV_D[27]	NAND Flash initialization sequence disable
	0 = If DEV_D[25] is set to 1 and DEV_D[27] is clear to 0, the NAND Flash initialization sequence is performed. 1 = The NAND Flash initialization sequence is disabled. **NOTE:** Internally pulled down to 0.
DEV_D[29:28]	Reserved for future use.
	Reserved Must be sampled at 0. **NOTE:** Internally pulled down to 0.
DEV_D[31:30]	Reserved for future use.
	Reserved

Note

Reset sampled values are registered in MPP Sample At Reset Register. See Table 270, “MPP Sample At Reset Register,” on page 249.

Part of the PCI interface signals are also sampled on PCI reset de-assertion, as specified in the PCI specification.

Table 22: PCI Reset Configuration

Pin	Configuration Function
PCI_REQ64n	PCI 64-bit enable
	0 = Enabled (PCI is working in 64-bit mode.) 1 = Disabled (PCI is working in 32-bit mode.)
PCI_M66EN	PCI 66 MHz enable
	0 = Disabled (For conventional PCI up to 37.5 MHz.) 1 = Enabled **NOTE:** Relevant only to conventional PCI mode.
PCI_DEVSELn PCI_STOPn PCI_TRDYn	PCI mode
	111 = Conventional PCI 110 = 66 MHz PCI-X 101 = 100 MHz PCI-X 100 = 133 MHz PCI-X All other combinations are reserved.

Note When configured to 32-bit PCI (PCI_REQ64n sampled high), the 88F5281 device constantly drives the upper side of the PCI bus (PCI_AD[63:32], PCI_CBEn[7:4], and PCI_PAR64).

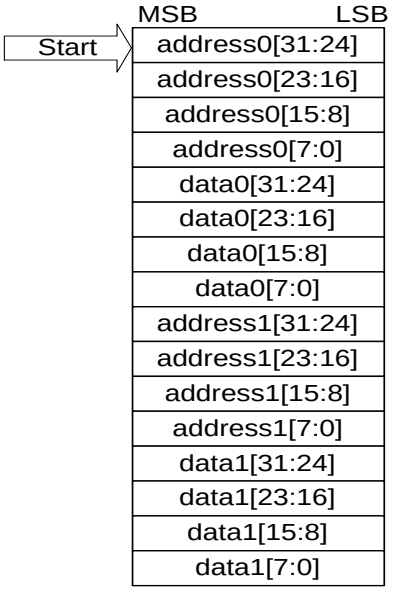
5.6 Serial ROM Initialization

The 88F5281 device supports initialization of ALL of its internal and configuration registers through the TWSI master interface. If serial ROM initialization is enabled, the 88F5281 device TWSI master starts reading initialization data from serial ROM and writes it to the appropriate registers.

5.6.1 Serial ROM Data Structure

Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 5.

Figure 5: Serial ROM Data Structure



The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target. This scheme enables not only programming of the 88F5281 internal registers, but

also initialization of other system components. The only limitation is that it supports only single 32-bit writes (no byte enables nor bursts are supported).

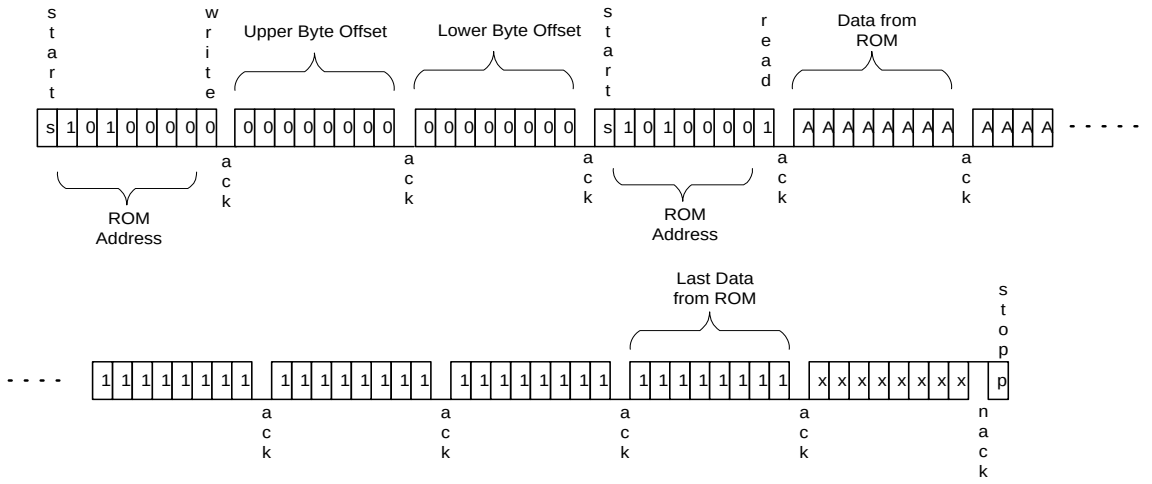
The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the 88F5281 device reaches last data, it stops the initialization sequence.

Note Users must not generate requests through the TWSI auto-loader to addresses that are not 32-bit aligned.

5.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the 88F5281 device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs the sequence of reads, until it reaches last data item, as shown in Figure 6.

Figure 6: Serial ROM Read Example



For a detailed description of TWSI implementation, see the Two-Wire Serial Interface section in the *88F5281 Datasheet Users Manual*.

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The 88F5281 device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the 88F5281 device receives an additional byte of dummy data. It responds with no-ack and then asserts the stop bit.

Note The read sequence above is a combined sequence. The service processor drives the start bit of the read access right after the acknowledge bit of last write access. TWSI Port1 also tolerates a none combined access. The service processor generates a stop bit at the end of the write access, only then does it issue the read access (this is the way FireFox TWSI works).

5.7 Power Sequencing

Refer to *AN-123 Power Sequencing for Marvell Devices,* Rev. A (Doc. No. MV-S300427-00).

6 Electrical Specifications (Preliminary)

The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

6.1 Absolute Maximum Ratings

Table 23: Absolute Maximum Ratings

Symbol	Min	Max	Units	Parameter
VDD_CORE	-0.5	1.5	V	Core voltage
VDD_CPU	-0.5	1.7	V	CPU core voltage
VDD_M	-0.5	3.0	V	I/O voltage for: DDR1/DDR2 SDRAM interface (SSTL)
M_SSTL_ VREF	-0.5	1.5	V	Reference voltage for: DDR1/DDR2 SDRAM interface (SSTL)
VDDO	-0.5	4.0	V	I/O voltage for: Device, PCI, MPP, JTAG, TWSI, UART Interfaces and CORE_REF_CLK, CPU_REF_CLK, and USB_REF_CLK
PEX_AVDDT	-0.5	1.8	V	Analog power supply voltage 1 for: PCI Express PHY
PEX_AVDDL	-0.5	1.8	V	Analog power supply voltage 2 for: PCI Express PHY
PEX_AVDD	-0.5	3.0	V	Analog power supply voltage 3 for: PCI Express PHY
PCI_AVDD[1]	-0.5	1.5	V	Analog power supply voltage for: PCI DLL
VDD_GE	-0.5	4.0	V	I/O voltage for: RGMII/GMII/MMII/MII interface
USB_AVDD	-0.5	4.0	V	I/O voltage for: USB interface
S_AVDD	-0.5	4.0	V	Quiet power supply for: CPU PLL
T_AVDD	-0.5	4.0	V	Quiet power supply for: Core PLL
TC	-40	125	° C	Case temperature
TSTG	-40	125	° C	Storage temperature

1. Input voltage must not exceed the respective interface supply voltage more than 0.7V.

Caution

- Exposure to conditions at or beyond the maximum rating may damage the device.
- Operation beyond the recommended operating conditions (Table 24) is neither recommended nor guaranteed.

Note

Before designing a system, it is recommended that you read application note AN-63: Thermal Management for Marvell Technology Products. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

6.2 Recommended Operating Conditions

Table 24: Recommended Operating Conditions

Symbol	Min	Typ	Max	Units	Parameter
VDD_CORE	1.14	1.2	1.26	V	Core voltage
VDD_CPU	1.34	1.4	1.45	V	CPU core voltage at 500 MHz
	1.14	1.2	1.26	V	CPU core voltage at 400 MHz
VDD_M	2.30	2.5	2.70	V	I/O voltage for: DDR1 SDRAM interface
	1.7	1.8	1.9	V	I/O voltage for: DDR2 SDRAM interface
M_SSTL_ VREF	0.49* VDD_M	0.5* VDD_M	0.51* VDD_M	V	Reference voltage for: DDR2 SDRAM interface
VDDO	3.15	3.3	3.45	V	I/O voltage for: Device, PCI, MPP, JTAG, TWSI, UART interfaces and CORE_REF_CLK, CPU_REF_CLK, and USB_REF_CLK
PEX_AVDDT	1.42	1.5	1.575	V	Analog power supply voltage 1 for: PCI Express PHY
PEX_AVDDL	1.42	1.5	1.575	V	Analog power supply voltage 2 for: PCI Express PHY
PEX_AVDD	2.38	2.5	2.62	V	Analog power supply voltage 3 for: PCI Express PHY
PCI_AVDD	1.14	1.2	1.26	V	Analog power supply voltage for: PCI DLL
VDD_GE	3.15	3.3	3.45	V	I/O voltage for: GMII/MMII/MII interface
	2.38	2.5	2.62	V	I/O voltage for: RGMII interface
USB_AVDD	3.15	3.3	3.45	V	I/O voltage for: USB interface
S_AVDD	3.15	3.3	3.45	V	Quiet power supply for: CPU PLL
T_AVDD	3.15	3.3	3.45	V	Quiet power supply for: Core PLL
	2.38	2.5	2.62	V	
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

6.3 Thermal Power Dissipation

Table 25: Thermal Power Dissipation

Interface	Symbol	Test Conditions	Typ	Units
Core	P_{VDD_CORE}		570	mW
CPU @ 500 MHz	P_{VDD_CPU}	VDD_CPU = 1.4V	3000	mW
CPU @ 400 MHz	P_{VDD_CPU}	VDD_CPU = 1.2V	2100	mW
CPU Standby Power	$P_{VDD\_CPU\_WFI}$	CPU in Wait for Interrupt (WFI)[3] state VDD_CPU = 1.4V CPU @ 500 MHz	280	mW
RGMII 2.5V interface	P_{VDD_GE}		50	mW
DDR1 DIMM interface parallel termination (32-bit 166 MHz)	P_{VDD_M}	2 single DIMM load	750	mW
DDR2 DIMM interface (32-bit 200 MHz) ODT	P_{VDD_M}	2 single DIMM load, 75 ohm ODT load	750	mW
PCI-X (133 MHz 64-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	P_{VDDO}		500	mW
PCI (66 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	P_{VDDO}	25 pF load	350	mW
PCI (33 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	P_{VDDO}	25 pF load	250	mW
PCI Express interface	P_{PEX}	When the port is not shutdown	120	mW
USB interface	P_{USB}	When the port is not shutdown	120	mW

Notes:

1. Power in mW is calculated using the typical recommended VDD specification for each power rail.
2. Trace load is 5 pF unless specified otherwise.
3. Wait for Interrupt (WFI): This instruction sets the CPU in Power Saving mode. The CPU confirms that the write buffer drained, the bus completed all pending transaction, and all further requests onto the bus are blocked before putting the CPU into Sleep mode. The CPU resumes regular operation upon receiving either an IRQ or FIQ interrupt.

   Refer to Marvell® Field Application Engineers (FAEs) or representatives for further information.

6.4 Current Consumption

Table 26: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core Digital Power Supply Current	I_{VDD_CORE}		475	mA
CPU Digital Power Supply Current @ 500 MHz	I_{VDD_CPU}	VDD_CPU = 1.45V	2200	mA
CPU Digital Power Supply Current @ 400 MHz	I_{VDD_CPU}	VDD_CPU = 1.26V	1550	mA
RGMII 2.5V interface	I_{VDD_GE}		50	mA
DDR1 DIMM interface parallel termination (32-bit 166 MHz)	I_{VDD_M}	2 single DIMM load	800	mA
DDR2 DIMM interface (32-bit 200 MHz) ODT	I_{VDD_M}	2 single DIMM load, 75 ohm ODT load	650	mA
PCI-X (133 MHz 64-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	I_{VDDO}		500	mA
PCI (66 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	I_{VDDO}	25 pf load	350	mA
PCI (33 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	I_{VDDO}	25 pf load	200	mA
PCI Express interface	I_{PEX_AVDD}	When the port is not shutdown	20	mA
	I_{PEX_AVDDL}		20	mA
	I_{PEX_AVDDT}		20	mA
PCI DLL	I_{PCI_AVDD}		10	mA
CPU PLL	I_{S_AVDD}		10	mA
Core PLL	I_{T_AVDD}		10	mA
USB interface	I_{USB}	When the port is not shutdown	40	mA

Notes:

1. Current in mA is calculated using maximum recommended VDD specification for each power rail.
2. All output clocks toggling at their specified rate.
3. Maximum drawn current from the power supply.
4. Trace load is 5 pF unless specified otherwise.

6.5 DC Electrical Specifications

6.5.1 Reduced Gigabit Media Independent Interface (RGMII) 2.5V DC Electrical Specifications

Table 27: RGMII Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 1 mA	-		0.4	V	-
Output high level	VOH	IOH = -1 mA	2		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.2 Gigabit Media Independent Interface (GMII) 3.3V DC Electrical Specifications

Table 28: GMII Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.3 Media Independent Interface (MII/MMII) 3.3V DC Electrical Specifications

Table 29: MII/MMII Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.4 Serial Management Interface (SMI) 3.3V DC Electrical Specifications

Table 30: SMI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.5 SDRAM DDR1 Interface 2.5V DC Electrical Specifications

Table 31: SDRAM DDR1 (DIMM) Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		VREF-0.15	V	-
Input high level	VIH		VREF+0.15		VDDIO+0.3	V	-
Output low level	VOL	IOL = 16.2 mA	-		0.35	V	-
Output high level	VOH	IOH = -16.2 mA	1.95		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.6 SDRAM DDR2 (DIMM) Interface 1.8V DC Electrical Specifications

Table 32: SDRAM DDR2 (DIMM) Interface 1.8V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL	-	-0.3		VREF - 0.125	V	-
Input high level	VIH	-	VREF + 0.125		VDDIO + 0.3	V	-
Output low level	VOL	IOL = 13.4 mA			0.28	V	-
Output high level	VOH	IOH = -13.4 mA	1.42			V	-
Rtt effective impedance value	RTT	See note 2	120	150	180	ohm	1 , 2
			60	75	90	ohm	1 , 2
			40	50	60	ohm	1 , 2
Deviation of VM with respect to VDDQ/2	dVm	See note 3	-6		6	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply VREF +/- 0.25 to input pin separately,
   then measure current $I_{(VREF\ +0.25)}$ and $I_{(VREF\ -0.25)}$ respectively.

$$RTT = \frac{0.5}{I_{(VREF\ +0.25)} - I_{(VREF\ -0.25)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1 \right) \times 100\,\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.7 PCI Interface 3.3V DC Electrical Specifications

Table 33: PCI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.5*VDDIO		VIO+0.5	V	-
Output low level	VOL	IOL = 1.5 mA	-		0.1*VDDIO	V	-
Output high level	VOH	IOH = -0.5 mA	0.9*VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.8 PCI-X Interface 3.3V DC Electrical Specifications

Table 34: PCI-X Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.35*VDDIO	V	-
Input high level	VIH		0.5*VDDIO		VIO+0.5	V	-
Output low level	VOL	IOL = 1.5 mA	-		0.1*VDDIO	V	-
Output high level	VOH	IOH = -0.5 mA	0.9*VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.9 UART Interface 3.3V DC Electrical Specifications

Table 35: UART Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.10 Device Bus 3.3V DC Electrical Specifications

Table 36: Device Bus 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.11 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

Table 37: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.12 JTAG Interface 3.3V DC Electrical Specifications

Table 38: JTAG Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

6.6 AC Electrical Specifications

See Section 6.7, Differential Interface Electrical Characteristics, on page 94 for differential interface specifications.

6.6.1 Reference Clock AC Timing Specifications

Table 39: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Core Reference Clock					
Frequency	$F_{CORE\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{CORE\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{CORE\_REF\_CLK}$		200	ps	
Slew rate	$SR_{CORE\_REF\_CLK}$	0.7		V/ns	1
Core Reference Clock Spread Spectrum Requirements					
Frequency Modulation	$Fmod_{CORE\_REF\_CLK}$	0	33	kHz	
F Spread	$Fspread_{CORE\_REF\_CLK}$	-1	0	%	
CPU Reference Clock					
Frequency	$F_{CPU\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{CPU\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{CPU\_REF\_CLK}$		200	ps	
Slew rate	$SR_{CPU\_REF\_CLK}$	0.7		V/ns	1
CPU Reference Clock Spread Spectrum Requirements					
Frequency Modulation	$Fmod_{CPU\_REF\_CLK}$	0	33	kHz	
F Spread	$Fspread_{CPU\_REF\_CLK}$	-1	0	%	
USB Reference Clock					
Frequency	$F_{USB\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{USB\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{USB\_REF\_CLK}$		200	ps	
Slew rate	$SR_{USB\_REF\_CLK}$	0.7		V/ns	1
Ethernet Reference Clocks					
Frequency in RGMII mode	$F_{RGE\_CLK\_125}$	125 - 50 ppm	125 + 50 ppm	MHz	

Table 39: Reference Clock AC Timing Specifications (Continued)

Description	Symbol	Min	Max	Units	Notes
Frequency in GMII mode	$F_{GGE\_CLK\_125}$	125 - 100 ppm	125 + 100 ppm	MHz	
Frequency in MII 100 Mbps MAC mode	F_{GE_RXCLK} F_{GE_TXCLK}	25 - 100 ppm	25 + 100 ppm	MHz	
Frequency in MII 10 Mbps MAC mode	F_{GE_RXCLK} F_{GE_TXCLK}	2.5 - 100 ppm	2.5 + 100 ppm	MHz	
Frequency in MMII MAC mode	F_{GE_RXCLK} F_{GE_TXCLK}	50 - 100 ppm	50 + 100 ppm	MHz	
Clock duty cycle	$DC_{GE\_CLK\_125}$	45	55	%	
Slew rate	$SR_{GE\_REF\_CLK}$	0.7		V/ns	1
SMI Master Mode Reference Clock					
SMI output MDC clock	F_{GE_MDC}	Core-Clock/128		MHz	
PCI In Clock					
Frequency	F_{PCLK}		33/66/133	MHz	3, 4
TCLK_OUT Out Clock					
Frequency	F_{TCLK_OUT}		166	MHz	
Clock duty cycle	DC_{TCLK_OUT}	40	60	%	2

Notes:

1. Slew rate is measured from 20% to 80% of the reference clock signal.
2. The load is CL = 15 pF.
3. Refer to Section 6.6.8, PCI Interface AC Timing, on page 84 for measurement and test conditions.
4. The PCI clock frequency is related to the PCI mode (see the <PCI_M66EN> field in Table 22, PCI Reset Configuration, on page 50).

Figure 7: 88F5281 TCLK_OUT Test Circuit

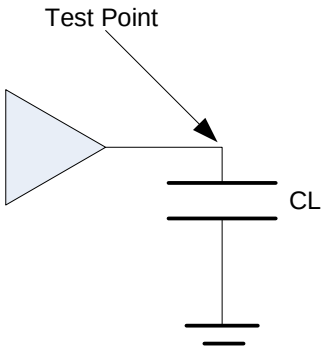
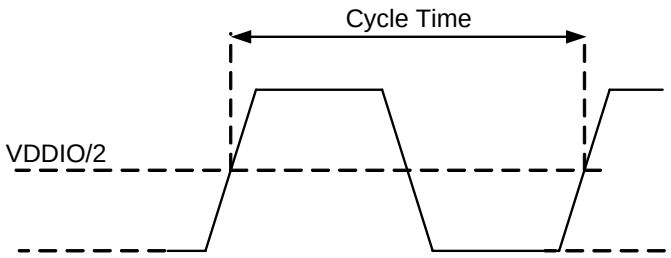


Figure 8: 88F5281 TCLK_OUT AC Timing Diagram



6.6.2 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

6.6.2.1 RGMII AC Timing Table

Table 40: RGMII- ID (PHY Internal Delay) AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	125.00		MHz	-
Data to Clock output skew (at transmitter)	TskewT	-0.50	0.50	ns	2
Data to Clock input setup (at receiver –integrated delay)	TsetupR	1.00	-	ns	-
Data to Clock input hold (at receiver –integrated delay)	TholdR	1.00	-	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

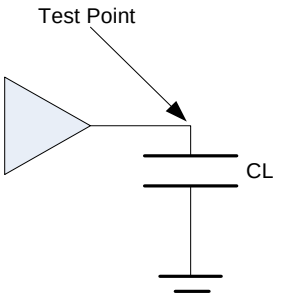
General comment: tCK = 1/fCK.

1. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns respectively.

2. For all signals the load is CL = 5 pF.

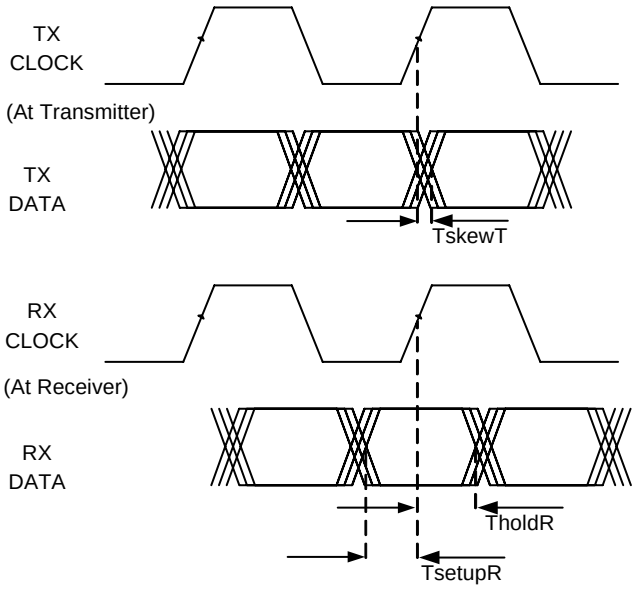
6.6.2.2 RGMII Test Circuit

Figure 9: RGMII Test Circuit



6.6.2.3 RGMII AC Timing Diagram

Figure 10: RGMII-ID (PHY Internal Delay) AC Timing Diagram



6.6.3 Gigabit Media Independent Interface (GMII) AC Timing

In this section, the signal names GTX_CLK and RX_CLK are referred to as GE_TXCLK and GE_RXCLK respectively, in the 88F5281.

6.6.3.1 GMII AC Timing Table

Table 41: GMII AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
GTX_CLK cycle time	tCK	7.5	8.5	ns	-
RX_CLK cycle time	tCKrx	7.5	-	ns	-
GTX_CLK and RX_CLK high level width	tHIGH	2.5	-	ns	1
GTX_CLK and RX_CLK low level width	tLOW	2.5	-	ns	1
GTX_CLK and RX_CLK rise time	tR	-	1.0	ns	1, 2
GTX_CLK and RX_CLK fall time	tF	-	1.0	ns	1, 2
Data input setup time relative to RX_CLK rising edge	tSETUP	2.0	-	ns	-
Data input hold time relative to RX_CLK rising edge	tHOLD	0.0	-	ns	-
Data output valid before GTX_CLK rising edge	tOVB	2.5	-	ns	1
Data output valid after GTX_CLK rising edge	tOVA	0.5	-	ns	1

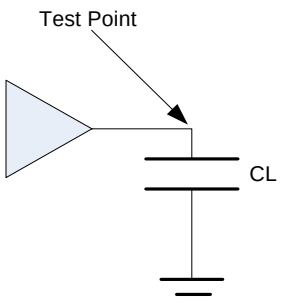
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

6.6.3.2 GMII Test Circuit

Figure 11: GMII Test Circuit



6.6.3.3 GMII AC Timing Diagrams

Figure 12: GMII Output Delay AC Timing Diagram

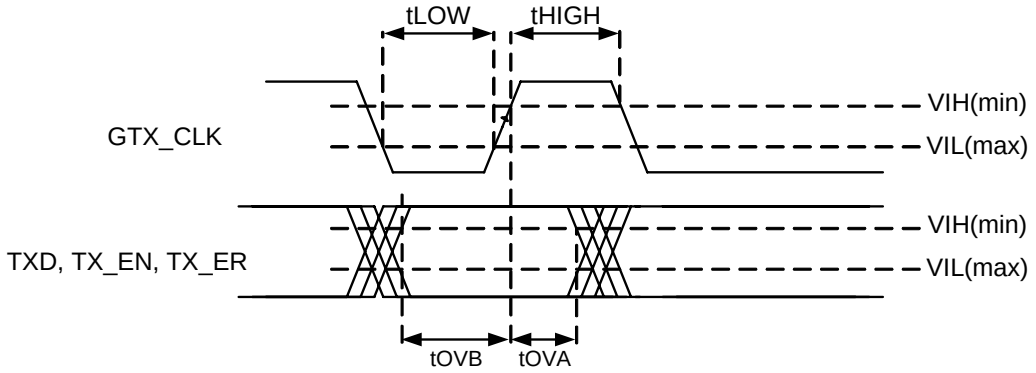
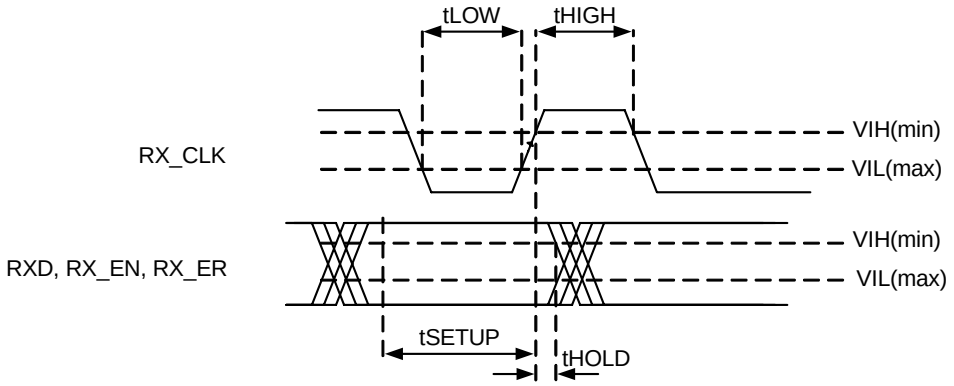


Figure 13: GMII Input AC Timing Diagram



6.6.4 Media Independent Interface (MII/MMII) AC Timing

6.6.4.1 MII/MMII PHY Mode AC Timing Table

Table 42: MII/MMII PHY Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

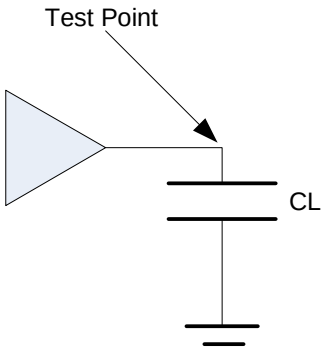
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

6.6.4.2 MII/MMII PHY Mode Test Circuit

Figure 14: MII/MMII PHY Mode Test Circuit



6.6.4.3 MII/MMII PHY Mode AC Timing Diagrams

Figure 15: MII/MMII PHY Mode Output Delay AC Timing Diagram

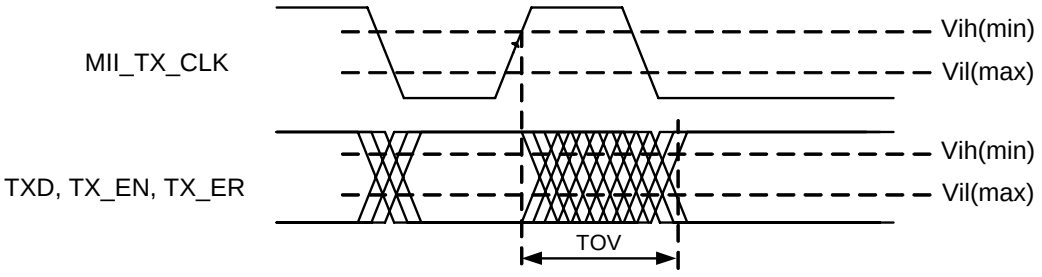
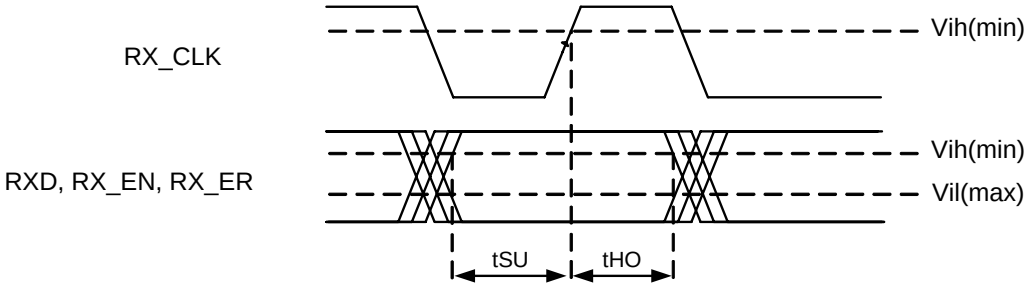


Figure 16: MII/MMII PHY Mode Input AC Timing Diagram



6.6.5 Serial Management Interface (SMI) AC Timing

In this section, the signal names MDC and MDIO are referred to as GE_MDC and GE_MDIO respectively, in the 88F5281.

6.6.5.1 SMI AC Timing Table

Table 43: SMI AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.40	0.60	tCK	-
MDIO input setup time relative to MDC rise time	tSU	40.00	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.00	-	ns	-
MDIO output valid before MDC rise time	tOVB	15.00	-	ns	1
MDIO output valid after MDC rise time	tOVA	15.00	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For MDC signal, the load is CL = 390 pF, and for MDIO signal, the load is CL = 470 pF.
2. See "Reference Clocks" table for more details.

6.6.5.2 SMI Test Circuit

Figure 17: MDIO Test Circuit

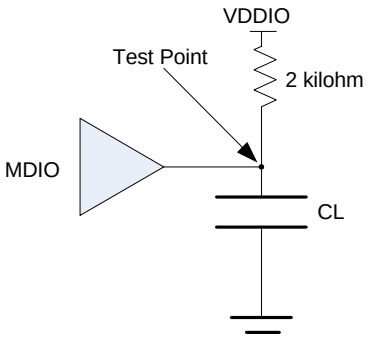
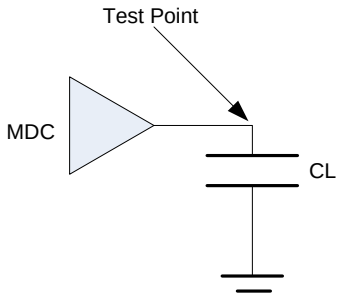


Figure 18: MDC Test Circuit



6.6.5.3 SMI AC Timing Diagrams

Figure 19: SMI Output Delay AC Timing Diagram

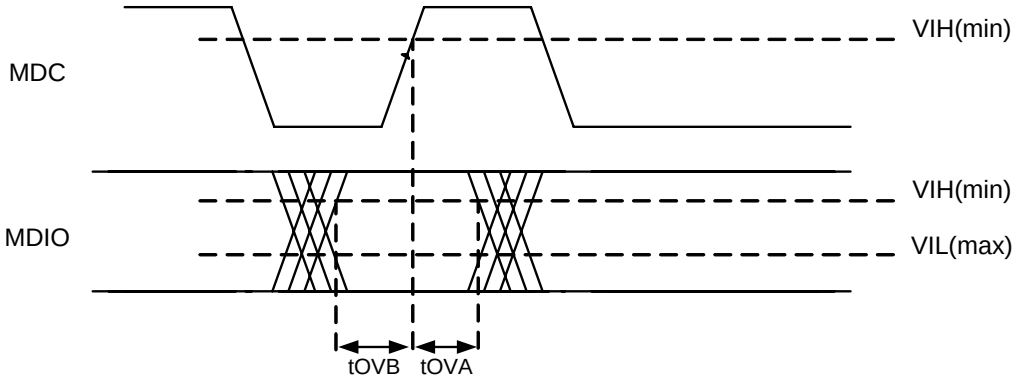
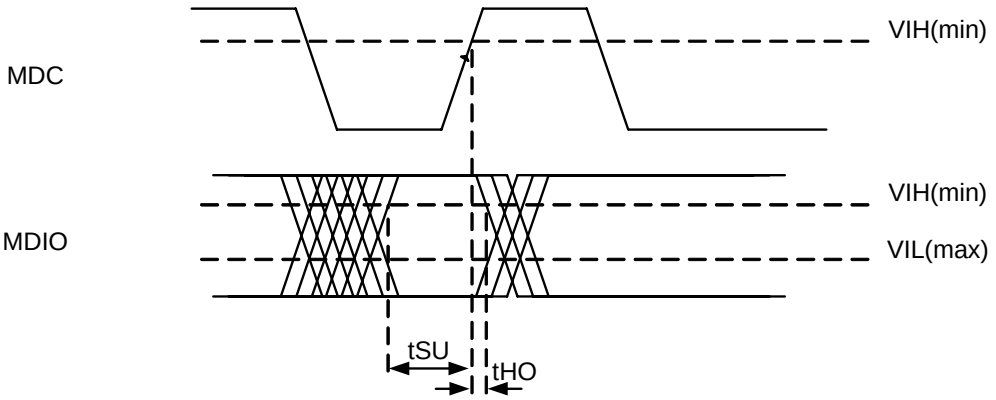


Figure 20: SMI Input AC Timing Diagram



6.6.6 SDRAM DDR1 32-bit Interface AC Timing

6.6.6.1 SDRAM DDR1 32-bit Interface AC Timing Table

Table 44: SDRAM DDR1 32-bit Interface AC Timing Table

Description	Symbol	166 MHz @ 2.5V		Units	Notes
		Min	Max		
Clock frequency	fCK	166.00		MHz	2
DQ and DM valid output time before DQS transition	tDOVB	0.55	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.55	-	ns	-
DQ and DM output pulse width	tDIPW	2.00	-	ns	-
DQS output high pulse width	tDQSH	0.37	-	tCK	-
DQS output low pulse width	tDQSL	0.37	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
Write command to first DQS latching transition	tDQSS	0.80	1.15	tCK	-
DQS write preamble	tWPRE	0.27	-	tCK	-
DQS write postamble	tWPST	0.43	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.55	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.90	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	3.50	-	ns	1, 3
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	1.00	-	ns	1, 3
Address and Control output pulse width	tIPW	4.80	-	ns	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-150 mV).

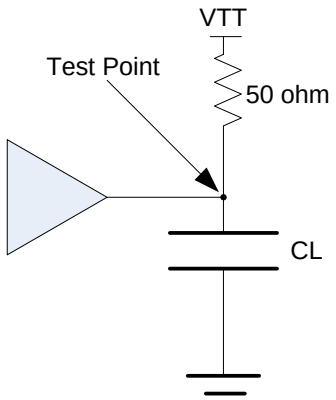
General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 22 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. Clock frequency is configurable. For more information, see register settings.
3. This timing value is defined when Address and Control signals are output ¼tCK after CLK-CLKn rising edge. For more information, see register settings.

6.6.6.2 SDRAM DDR1 32-bit Interface Test Circuit

Figure 21: SDRAM DDR1 32-bit Interface Test Circuit



6.6.6.3 SDRAM DDR1 32-bit Interface AC Timing Diagrams

Figure 22: SDRAM DDR1 32-bit Interface Write AC Timing Diagram

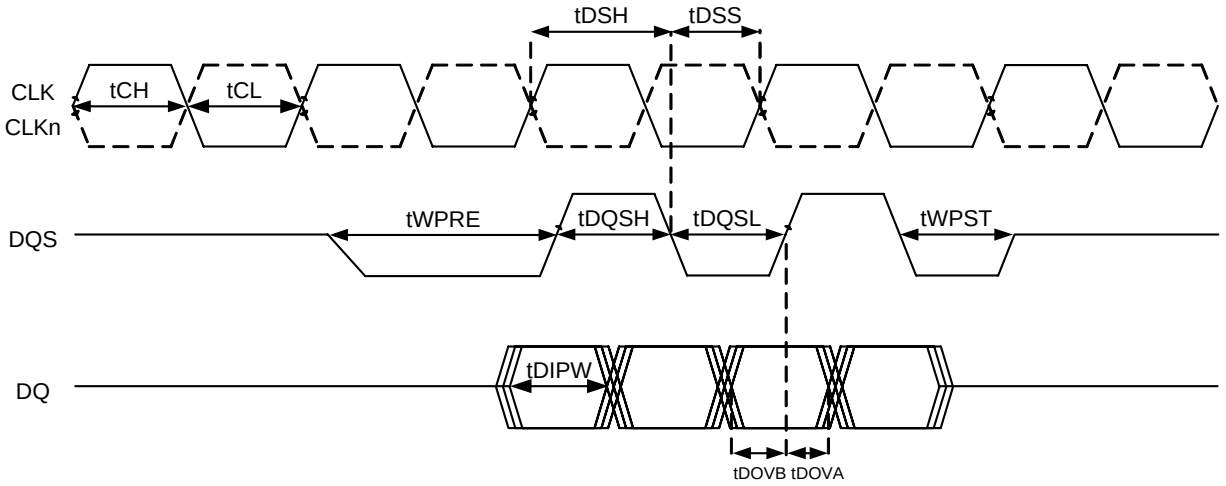


Figure 23: SDRAM DDR1 32-bit Interface Address and Control AC Timing Diagram

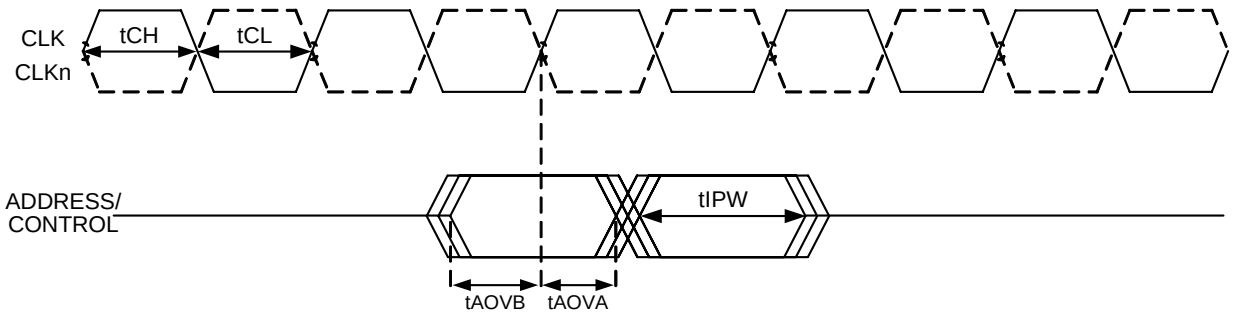
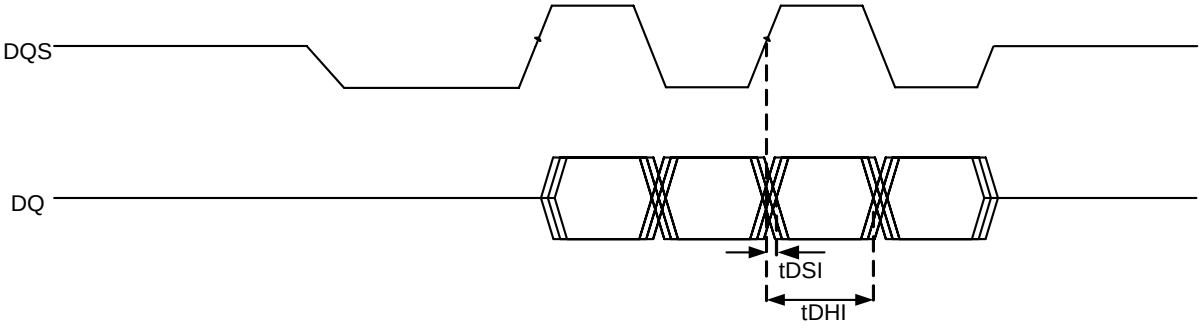


Figure 24: SDRAM DDR1 32-bit Interface Read AC Timing Diagram



6.6.7 SDRAM DDR2 32-bit Interface AC Timing

6.6.7.1 SDRAM DDR2 32-bit Interface AC Timing Table

Table 45: SDRAM DDR2 32-bit Interface AC Timing Table

Description	Symbol	200 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	200.00		MHz	3
DQ and DM valid output time before DQS transition	tDOVB	0.50	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.50	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK	-
DQS output high pulse width	tDQSH	0.35	-	tCK	-
DQS output low pulse width	tDQSL	0.35	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
Write command to first DQS latching transition	tDQSS	WL-0.25	WL+0.25	tCK	2
DQS write preamble	tWPRE	0.35	-	tCK	-
DQS write postamble	tWPST	0.41	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.55	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.50	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	2.25	-	ns	1, 4
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.70	-	ns	1, 4
Address and control output pulse width	tIPW	0.67	-	tCK	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

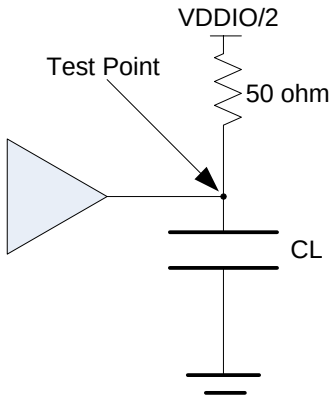
General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 16 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. WL = Write Latency.
3. Clock frequency is configurable. For more information, see register settings.
4. This timing value is defined when Address and Control signals are output ¼tCK after CLK-CLKn rising edge. For more information, see register settings.

6.6.7.2 SDRAM DDR2 32-bit Interface Test Circuit

Figure 25: SDRAM DDR2 32-bit Interface Test Circuit



6.6.7.3 SDRAM DDR2 32-bit Interface AC Timing Diagrams

Figure 26: SDRAM DDR2 32-bit Interface Write AC Timing Diagram

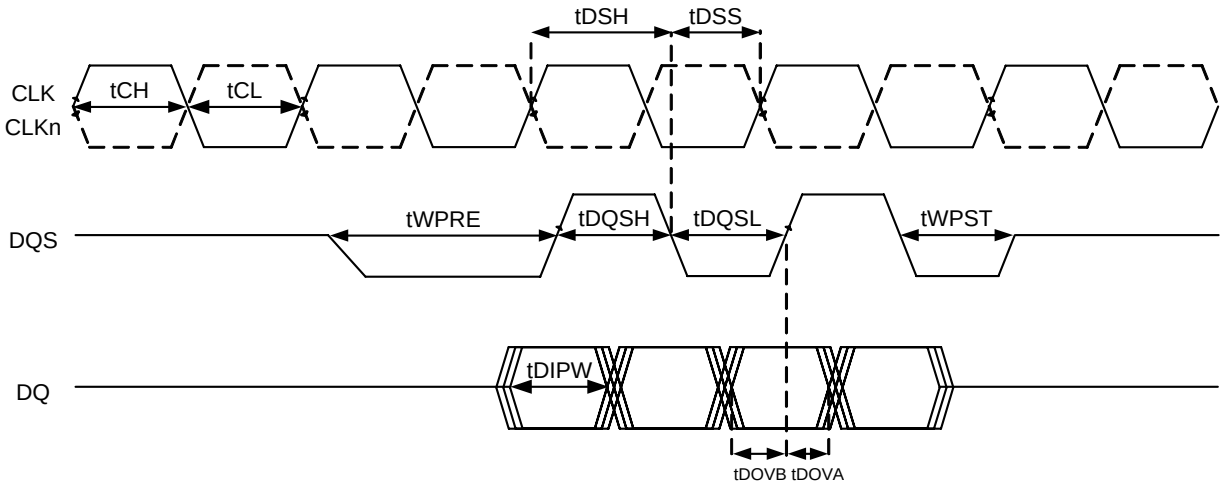


Figure 27: SDRAM DDR2 32-bit Interface Address and Control AC Timing Diagram

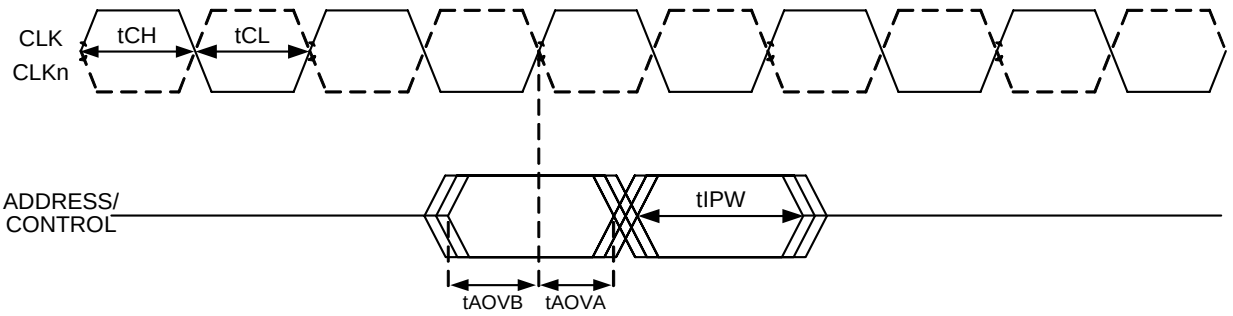
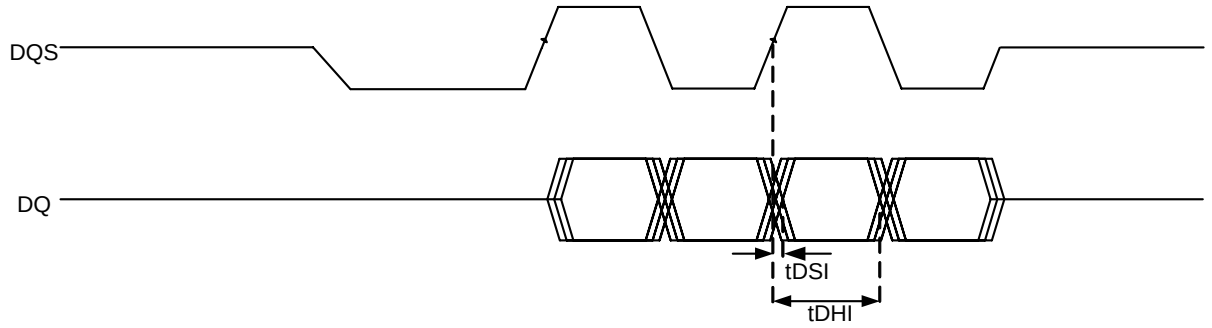


Figure 28: SDRAM DDR2 32-bit Interface Read AC Timing Diagram



6.6.8 PCI Interface AC Timing

6.6.8.1 PCI Interface AC Timing Table

Table 46: PCI/PCI-X Interface AC Timing Table

Description	Symbol	PCI-X 133 MHz @ 3.3V		PCI-X 100 MHz @ 3.3V		PCI-X 66 MHz @ 3.3V		PCI 66 MHz @ 3.3V		PCI 33 MHz @ 3.3V		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock cycle time	Tcyc	7.5	20.0	10.0	20.0	15.0	20.0	15.0	30.0	30.0	-	ns	1
Clock high time	Thigh	3.0	-	4.0	-	6.0	-	6.0	-	11.0	-	ns	-
Clock low time	Tlow	3.0	-	4.0	-	6.0	-	6.0	-	11.0	-	ns	-
Clock slew rate	-	1.5	4.0	1.5	4.0	1.5	4.0	1.5	4.0	1.0	4.0	V/ns	2
Clock rising edge to signal valid delay for bused signals	Tval	0.7	3.8	0.7	3.8	0.7	3.8	2.0	6.0	2.0	11.0	ns	3, 4
Clock rising edge to signal valid delay for point to point signals	Tval(ptp)	0.7	3.8	0.7	3.8	0.7	3.8	2.0	6.0	2.0	12.0	ns	3, 4
Input setup time to Clock rising edge for bused signals	Tsu	1.2	-	1.2	-	1.7	-	3.0	-	7.0	-	ns	4, 6, 8
Input setup time to Clock rising edge for point to point signals	Tsu(ptp)	1.2	-	1.2	-	1.7	-	5.0	-	10, 12	-	ns	4, 5, 6
Input hold time from Clock rising edge	Th	0.5	-	0.5	-	0.5	-	0.0	-	0.0	-	ns	6
Reset active time	Trst	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ms	7
Output rise slew rate	tr	1.0	6.0	1.0	6.0	1.0	6.0	1.0	4.0	1.0	4.0	V/ns	9
Output fall slew rate	tf	1.0	6.0	1.0	6.0	1.0	6.0	1.0	4.0	1.0	4.0	V/ns	9

Notes:
1. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in the PCI Interface Clock waveform.
3. See the timing measurment conditions in the Output Timing Measurement Conditions figure.
4. Point-to-point signals applies to REQn and GNTn only. All other signals are bused.
5. For PCI 33 MHz: GNTn has a setup of 10 ns; REQn has a setup of 12 ns.
6. See the timing measurement conditions in the Input Timing Measurement Conditions figure.
7. RSTn is asserted and deasserted asynchronously with respect to Clock.
8. Setup time applies only when the device is not driving the pin.
   Devices cannot drive and receive signals at the same time.
9. The test load for PCI-X is specified in the Output Slew Rate Test Load figure,
   and the test load for PCI is specified in the Tval (Min) Test Load figure.

Table 47: PCI Clock Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	30.0	33.0	kHz	-
Fspread	-1.0	0.0	%	-

General comment: Relevant for PCI-X 133/100/66 MHz and Conventional PCI 66 MHz.

6.6.8.2 PCI Interface Test Circuit

Figure 29: Tval (Max) Rising Edge Test Load

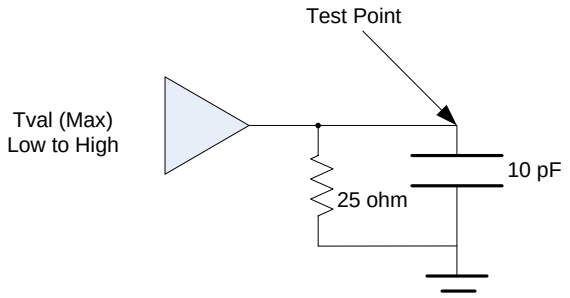


Figure 30: Tval (Max) Falling Edge Test Load

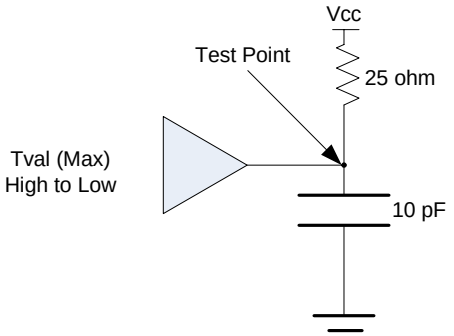


Figure 31: Tval (Min) Test Load & Output Slew Rate Test Load (for Conventional PCI)

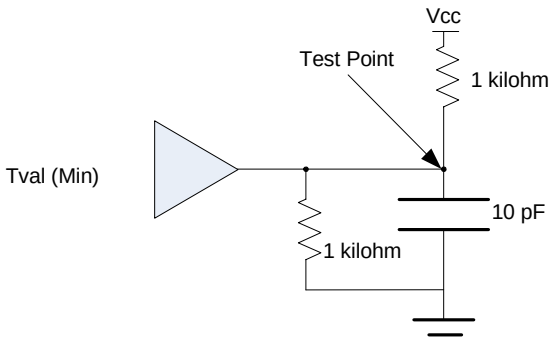
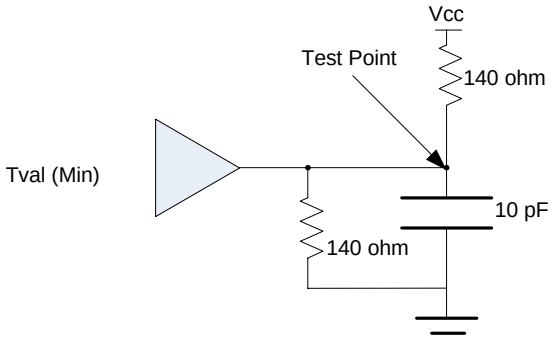


Figure 32: Output Slew Rate Test Load (for PCI-X only)



6.6.8.3 PCI Interface Measurement Condition Parameters

Table 48: PCI/PCI-X Interface Measurement Condition Parameters

Symbol	PCI-X	PCI	Units	Notes
Vth	0.6 Vcc	0.6 Vcc	V	-
Vtl	0.25 Vcc	0.2 Vcc	V	-
Vtest	0.4 Vcc	0.4 Vcc	V	-
Vtrise	0.285 Vcc	0.285 Vcc	V	1
Vtfall	0.615 Vcc	0.615 Vcc	V	1
Output rise slew rate	0.3 Vcc to 0.6 Vcc		V	-
Output fall slew rate	0.6 Vcc to 0.3 Vcc		V	-
Input signal slew rate	1.5	1.5	V/ns	2

Notes:
1. Vtrise and Vtfall are reference voltages for timing definitions only.
2. Input signal slew rate in PCI-X mode is defined between Vil and Vih.

6.6.8.4 PCI Interface AC Timing Measurement Waveforms

Figure 33: PCI Interface Clock Waveform

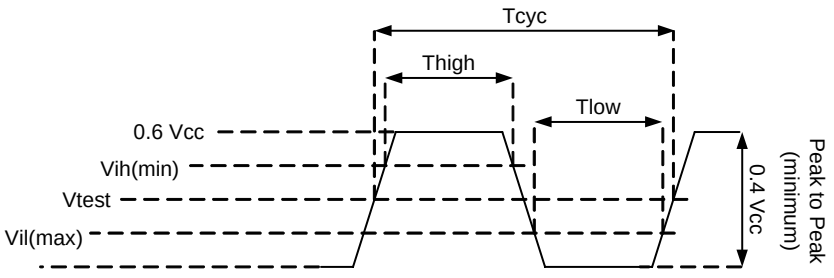


Figure 34: PCI Interface Output Timing Measurement Conditions

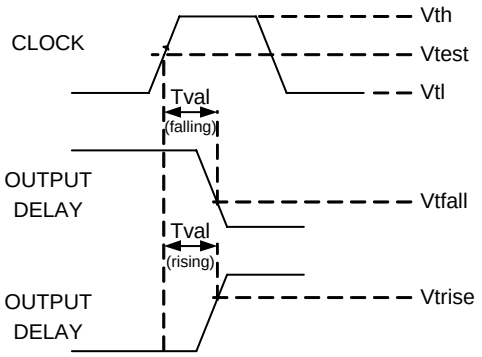
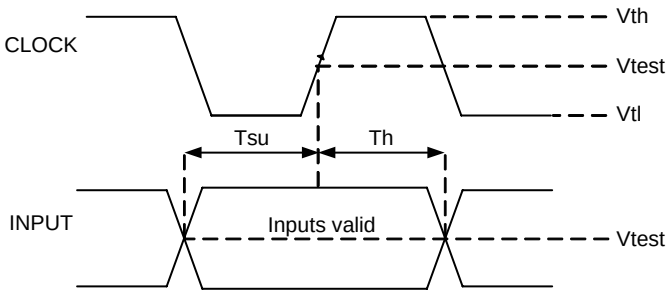


Figure 35: PCI Interface Input Timing Measurement Conditions



6.6.9 Device Bus Interface AC Timing

6.6.9.1 Device Bus Interface AC Timing Table

Note The device bus output clock is TCLK_OUT.

Table 49: Device Bus Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data/READYn input setup relative to clock rising edge	tSU	3.0	-	ns	-
Data/READYn input hold relative to clock rising edge	tHD	1.0	-	ns	-
Address/Data output delay relative to clock rising edge	tOV	0.8	3.5	ns	1
Address output valid before ALE signal falling edge	tAOAB	5.0	-	ns	1 , 2
Address output valid after ALE signal falling edge	tAOAA	5.0	-	ns	1 , 2

Notes:

General comment: All timing values are for interfacing synchronous devices.

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 10 pF.
2. The AD bus is normally loaded with high capacitance. Make sure to work according to HW design guide lines or simulations in order to meet the latch AC timing requirements.

6.6.9.2 Device Bus Interface Test Circuit

Figure 36: Device Bus Interface Test Circuit

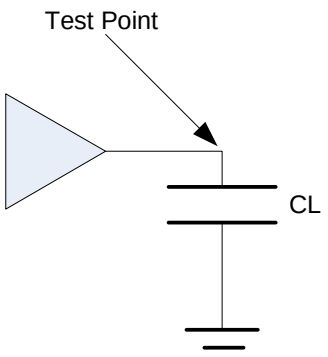


Figure 37: Device Bus Interface Output Delay AC Timing Diagram

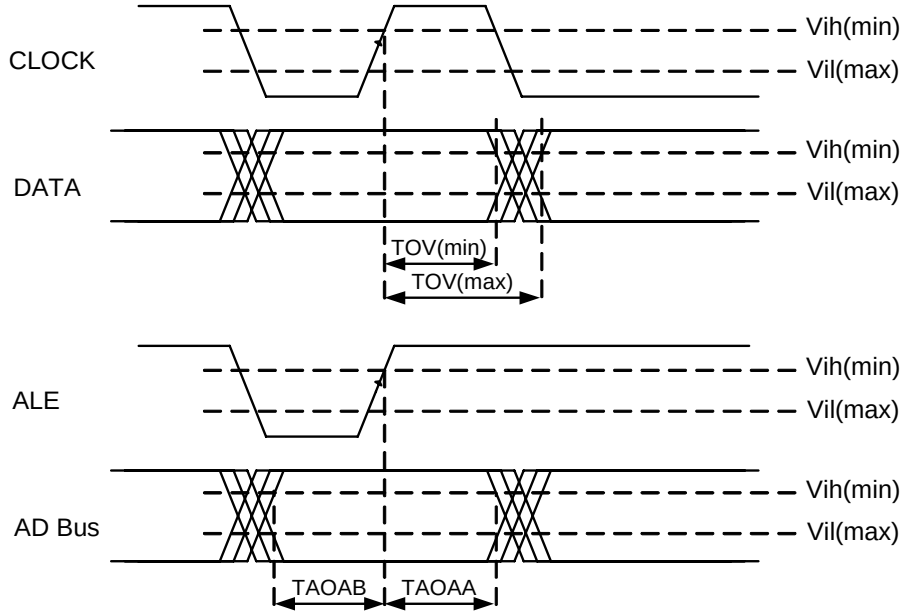
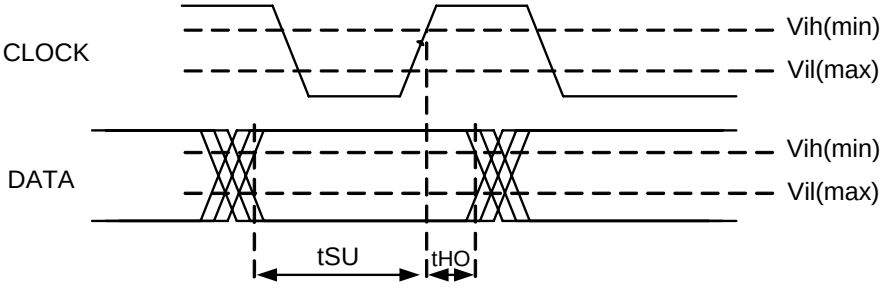


Figure 38: Device Bus Interface Input AC Timing Diagram



6.6.10 Two-Wire Serial Interface (TWSI) AC Timing

6.6.10.1 TWSI AC Timing Table

Table 50: TWSI AC Timing Table

Description	Symbol	100 kHz		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK rising edge	tOV	4.0	7.0	us	1

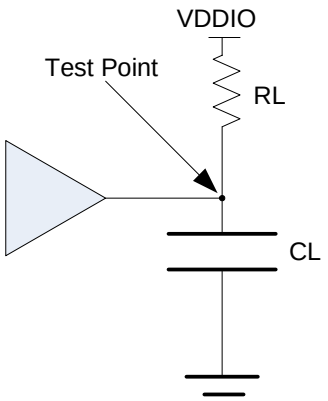
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

6.6.10.2 TWSI Test Circuit

Figure 39: TWSI Test Circuit



6.6.10.3 TWSI AC Timing Diagrams

Figure 40: TWSI Output Delay AC Timing Diagram

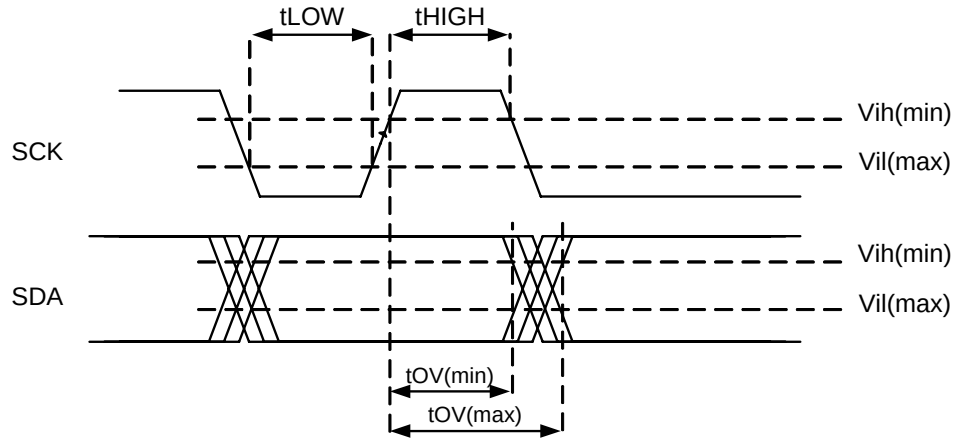
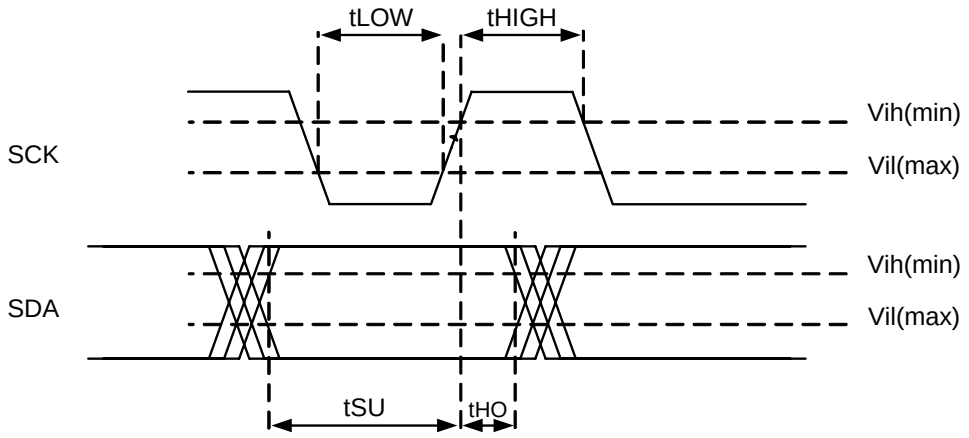


Figure 41: TWSI Input AC Timing Diagram



6.6.11 JTAG Interface AC Timing

6.6.11.1 JTAG Interface AC Timing Table

Table 51: JTAG Interface AC Timing Table

Description	Symbol	5 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	5.0		MHz	-
JTClk minimum pulse width	Tpw	0.40	0.60	tCK	-
JTClk rise/fall time	Tr/Tf	-	2.0	ns	2
JTRSTn active time	Trst	1.00	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	10.0	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	75.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	20.0	ns	1

Notes:

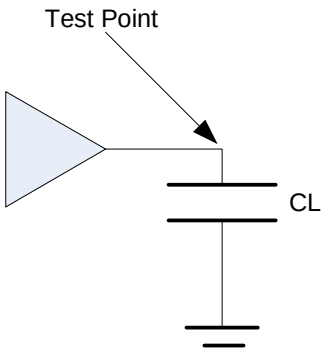
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 20 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

6.6.11.2 JTAG Interface Test Circuit

Figure 42: JTAG Interface Test Circuit



6.6.11.3 JTAG Interface AC Timing Diagrams

Figure 43: JTAG Interface Output Delay AC Timing Diagram

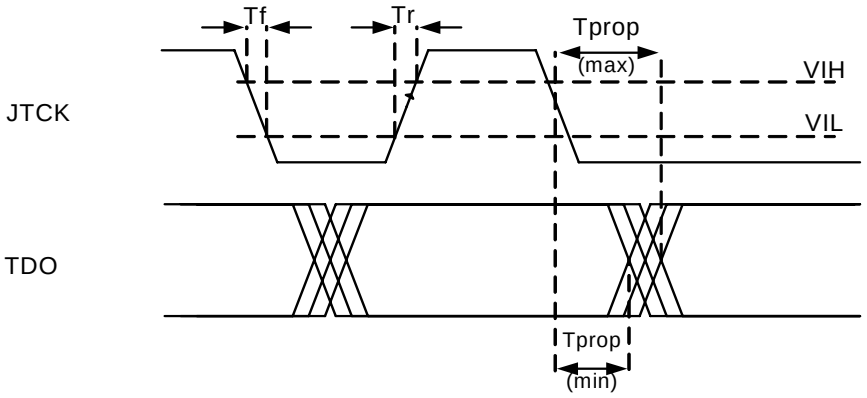
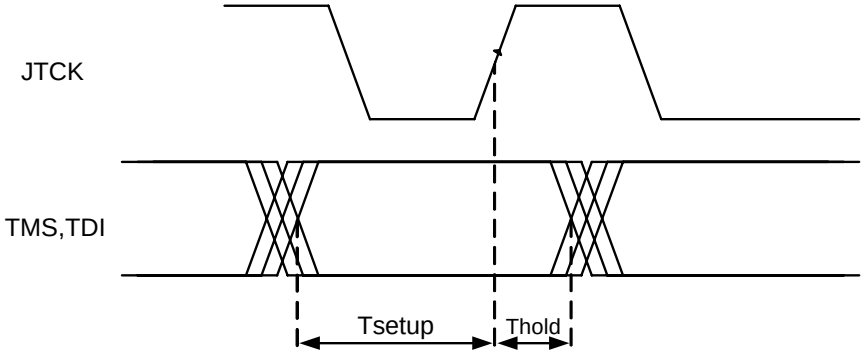


Figure 44: JTAG Interface Input AC Timing Diagram



6.7 Differential Interface Electrical Characteristics

This section provides the AC and DC characteristics for the PCI Express Interface Electrical Characteristics Differential interface.

The 88F5281 is compliant with the standards listed below. Refer to the respective interface electrical specifications for these interfaces:

USB interface — For Low/Full/High speed modes, refer to the *Universal Serial Bus Specification*, Revision 2.0, April 2000.

6.7.1 Differential Interface Reference Clock Characteristics

6.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

Table 52: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100.0		MHz	-
Clock duty cycle	DCrefclk	0.45	0.55	tCK	-
Clock rise/fall time	TRrefclk	175.0	700.0	pS	1, 3
Clock rise/fall time variation	dlTRrefclk	-	125.0	pS	1, 3
High voltage	VIHrefclk	660.0	850.0	mV	1
Low voltage	VILrefclk	-150.0	50.0	mV	1
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Absolute maximum input voltage (overshoot)	Vmax	-	1.15	V	1
Absolute minimum input voltage (undershoot)	Vmin	-	-0.3	V	1
Absolute differential clock period	Tperabs	9.872	-	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	125.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.0a, April 2003, section 2.6.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.
3. Defined from 0.175V to 0.525V.

6.7.2 PCI Express Interface Electrical Characteristics

6.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 53: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.7	-	UI	-
Differential return loss	TRLdiff	12.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	15.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.0a, April, 2003.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

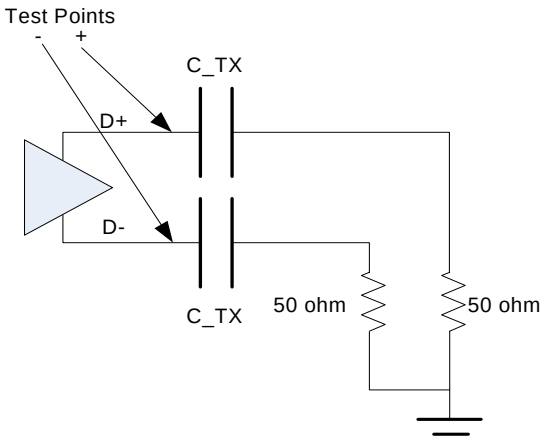
6.7.2.2 PCI Express Interface Spread Spectrum Requirements

Table 54: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	30.0	33.0	kHz	-
Fspread	-0.5	0.0	%	-

6.7.2.3 PCI Express Interface Test Circuit

Figure 45: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

7 Thermal Data

Note

- The following parameters are preliminary and subject to change.
- It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

7.1 88F5281 Thermal Data

Note

It is recommended to read application note AN-63 Thermal Management for Selected Marvell® Products (Document Number MV-S300281-00) and the ThetaJC, ThetaJA, and Temperature Calculations White Paper, available from Marvell, before designing a system. These documents describe basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 55 provides the thermal data for the 88F5281. The simulation was done according to JEDEC standards.

Table 55: Thermal Data for the 88F5281 in HSBGA426 Package

Symbol	Definition	Value per different air flows (m/s)			Unit
		0	1	2	
θ_{JA}	Thermal resistance: junction to ambient.	14.0	12.2	11.6	C/W
Ψ_{JT}	Thermal characterization parameter: junction to case center.	2.8	2.8	2.8	C/W
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	3.9			C/W
Ψ_{JB}	Thermal characterization parameter: junction to the bottom of the package.	6.5	6.4	6.3	C/W
θ_{JB}	Thermal resistance: junction to the bottom of the package (not air-flow dependent)	7.1			C/W

8 Package Mechanical Dimensions

The 88F5281 uses a 426-pin Heat Slug Ball Grid Array (HSBGA) 23 x 23 mm x 1.93 mm package.

Figure 46: HSBGA, 23x23 mm, 426-pin Package Diagram

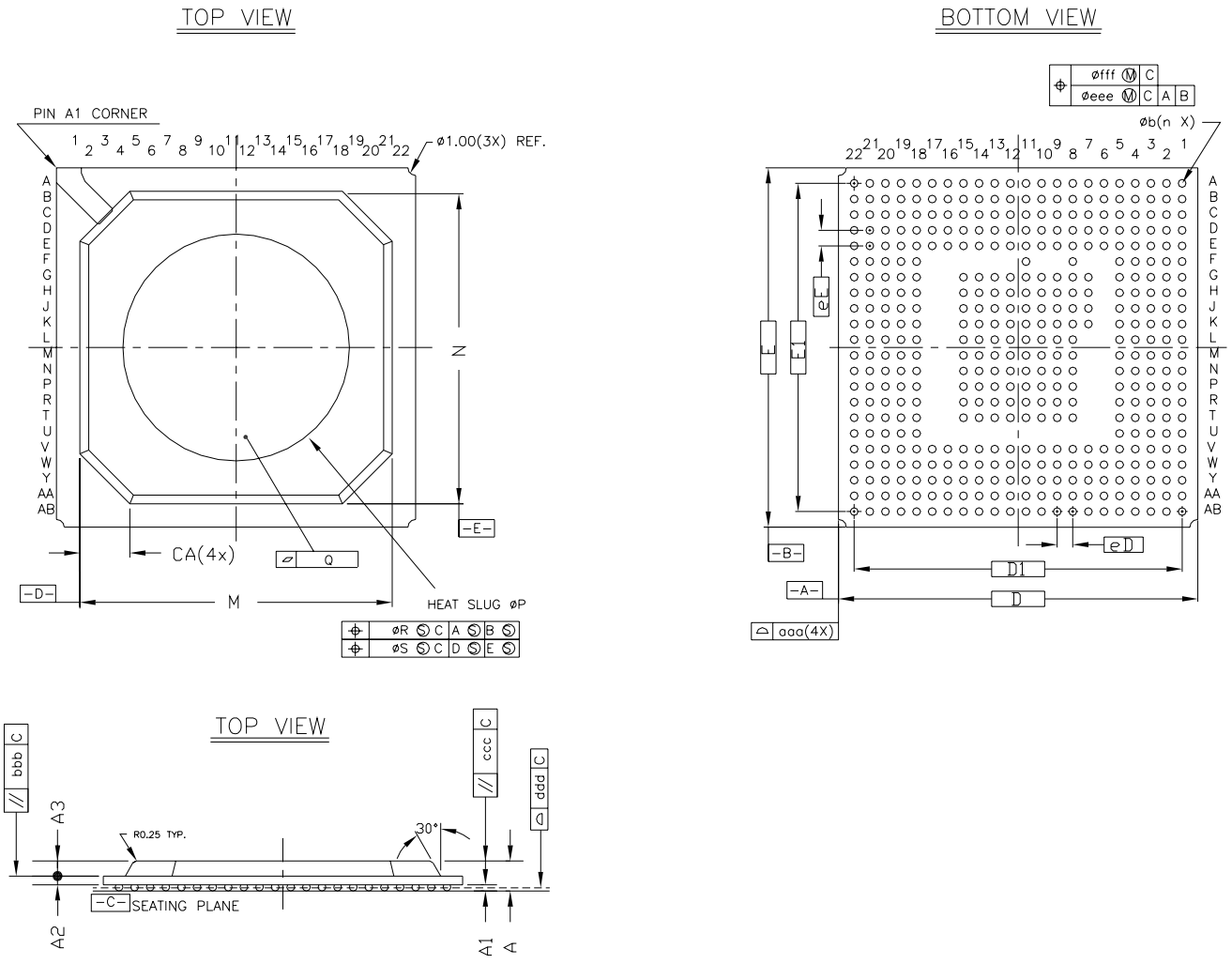


Table 56: Package Drawing Key

		Symbol	Common Dimensions
Package :			HS BGA
Body Size:	X	D	23.000
	Y	E	23.000
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	1.930 ± 0.130
Mold Thickness :		A3	0.970 Ref.
Substrate Thickness :		A2	0.560 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.300 ~ 0.500
Ball Width :		b	0.400 ~ 0.600
Mold Area :	X	M	20.000
	Y	N	20.000
H/S Exposed Size :		P	14.500 ~ 15.500
H/S Flatness :		Q	0.100
H/S Shift With Substrate Edge :		R	0.300
H/S Shift With Mold Area :		S	0.500
Chamfer		CA	3.200 REF.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.200
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	426
Edge Ball Center to Center :	X	D1	21.000
	Y	E1	21.000

9 Part Order Numbering/Package Marking

Figure 47 is an example of the part order numbering scheme for the 88F5281.

Figure 47: Sample Part Number

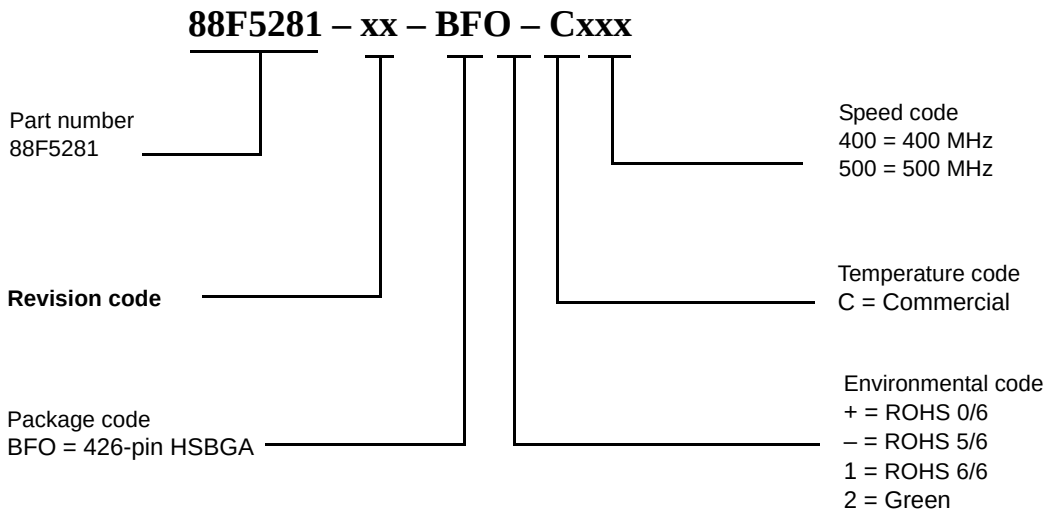
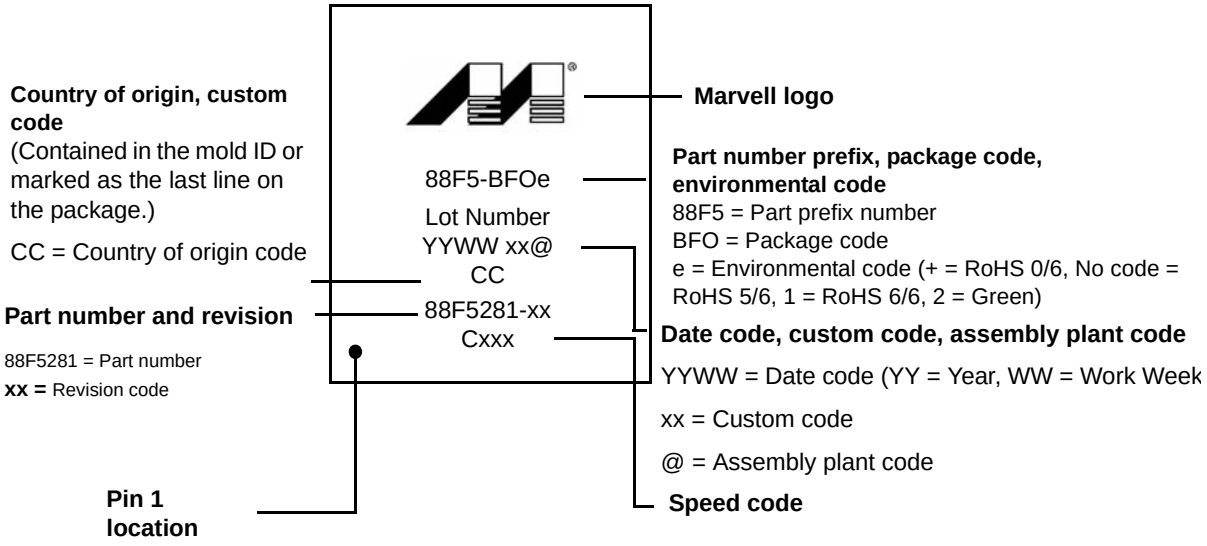


Table 57: 88F5281 Part Order Options

Package Type	Part Order Number
HSBGA (23x23 mm, 426-pin package) 400 MHz	88F5281-xx-BFO-C400 (ROHS 5/6 compliant package)
HSBGA (23x23 mm, 426-pin package) 400 MHz	88F5281-xx-BFO1C400 (ROHS 6/6 compliant package)
HSBGA (23x23 mm, 426-pin package) 400 MHz	88F5281-xx-BFO2C400 (Green compliant package)
HSBGA (23x23 mm, 426-pin package) 500 MHz	88F5281-xx-BFO-C500 (ROHS 5/6 compliant package)
HSBGA (23x23 mm, 426-pin package) 500 MHz	88F5281-xx-BFO1C500 (ROHS 6/6 compliant package)
HSBGA (23x23 mm, 426-pin package) 500 MHz	88F5281-xx-BFO2C500 (Green compliant package)

Figure 48 shows a sample package marking and pin 1 location for the 88F5281.

Figure 48: 88F5281 Package Marking and Pin 1 Location



Note: The above drawings are not drawn to scale. Location of markings is approximate.

A Revision History

Table 58: Revision History

Document Type	Rev	Date
Initial release	A	September 13, 2006
Revision	B	March 27, 2007
1. In Table 21, Reset Configuration, on page 47, reduced the list of reserved pins to: DEV_D[18].		
2. Revised Table 23, Absolute Maximum Ratings, on page 55 to state that for PCI_AVDD the input voltage must not exceed the respective interface supply voltage more than 0.7 V.		
3. Added the row CPU Standby Power to Table 25, Thermal Power Dissipation, on page 58 and added a description of Wait for Interrupt (WFI).		
4. In Table 39, Reference Clock AC Timing Specifications, on page 67, revised the description of F_{GE_RXCLK} and F_{GE_TXCLK} to state that the MII and MMII interfaces are in MAC mode.		
5. Revised the values for symbols tAOVB, tAOVA, and tIPW Table 44, SDRAM DDR1 32-bit Interface AC Timing Table, on page 78		
6. Revised the values for symbols tWPRE and tAOVB in Table 45, SDRAM DDR2 32-bit Interface AC Timing Table, on page 81 and added notes 3 and 4.		
7. In Table 51, “JTAG Interface AC Timing Table,” on page 90, changed the second parameter to JTClk minimum pulse width (symbol Tpw) and added the parameter JTClk rise/fall time (symbol Tr/Tf). Also added note 2.		
8. Revised Figure 43, “JTAG Interface Output Delay AC Timing Diagram,” on page 91.		
9. Revise the beginning of Section 6.7, Differential Interface Electrical Characteristics, on page 94 and added Section 6.7.1, Differential Interface Reference Clock Characteristics, on page 94 and Table 52, PCI Express Interface Differential Reference Clock Characteristics, on page 94.		
10. Revised Figure 48, 88F5281 Package Marking and Pin 1 Location, on page 101.		
Revision	C	June 7, 2007
1. In Table 4, PCI Express Interface Pin Assignments, on page 19 and Table 7, USB 2.0 Interface Pin Assignments, on page 26, added the power rail column.		
2. In Table 6, Gigabit Ethernet Port Interface Pin Assignments, on page 23, revise the power rail to VDDO for pins: GE_TXD[7:4], GE_TXERR, GE_CRS, GE_RXD[7:4], GE_RXERR, GE_COL.		
3. In Table 13, Miscellaneous Pin Assignments, on page 31, revised the description of SYSRSTn.		
4. At the beginning of Section 5.5, Pins Sample Configuration, on page 47, added two more notes about the pull-up/down resistor.		
5. In Table 21, Reset Configuration, on page 47, revised rows: DEV_A[2], DEV_D[18], DEV_D[20], DEV_D[21], DEV_D[20], DEV_D[29:28], and DEV_D[31:30].		
6. In Table 50, TWSI AC Timing Table, on page 90, revised the description of symbol tHD to indicate that it is relative to SCK falling edge and revised the minimum value of symbol tOV to 4.0 µs.		
7. Revised Figure 47, Sample Part Number, on page 100.		
8. Revised Figure 48, 88F5281 Package Marking and Pin 1 Location, on page 101.		
Revision	D	January 7, 2008
1. Revised Note in Table 5, PCI Bus Interface Pin Assignments, on page 20 to “All PCI pads are 5V tolerant when PCI_VIO is conncted to 5V.”		
2. In Table 6, Gigabit Ethernet Port Interface Pin Assignments, on page 23, added note to GE_MDIO description.		
3. In Table 7, USB 2.0 Interface Pin Assignments, on page 26, VBUS pin description changed to not connected.		

Table 58: Revision History (Continued)

Document Type	Rev	Date
4. In Section 1.2.6, TWSI Interface Pin Assignment, on page 27, added note: "When working with the TWSI interface, the TW_SDA and TW_SCK pins must be pulled up to VDDO".		
5. In Table 11, Device Bus Interface Pin Assignments, on page 29, added note and revised the description of DEV_WEn[3:0], DEV-OEn, DEV_D[7:0] and DEV_A[2:0].		
6. In Section 5.2.1, PCI Express Reset in Endpoint Mode, on page 45, added note: "When working in Endpoint mode, clear bits [16], [17], and [19] of the PCI Express register at offset 0x41A60".		
7. In Table 57, 88F5281 Part Order Options, on page 100, added Green part numbers.		
8. Revised Figure 47, Sample Part Number, on page 100.		
Revision	E	April 29, 2008
1. Changed document classification..		

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